Final Technical Report

TRANSIENT VELOCITY ASSESSMENT IN GALLIUM ARSENIDE, AND OF OTHER GaAs CHARACTERISTICS RELATED TO DEVICE FUNCTIONS

Sponsored by

Defense Advanced Research Projects Agency

Submitted by

J. S. Blakemore

Principal Investigator

and

R. E. Kremer

Faculty Associate

Oregon Graduate Center

19600 N.W. Von Neumann Dr.

Beaverton, OR 97006-1999

Final Technical Report

TRANSIENT VELOCITY ASSESSMENT IN GALLIUM ARSENIDE, AND OF OTHER GaAs CHARACTERISTICS RELATED TO DEVICE FUNCTIONS

Sponsored by

Defense Advanced Research Projects Agency
ARPA Order No. 5020/1
Program Code 4D10

Contract No. MDA903-84-K-0374, issued by
Dep't. of the Army, Defense Supply Service,
Washington, DC 20310

Administered by ONR: Seattle
Serial RW-809

Scientific Program Officer: Mr. Sven A. Roosild, DARPA/DSO
1400 Wilson Blvd.
Arlington, VA 22209

Contractor: Oregon Graduate Center
19600 NW Von Neumann Dr.
Beaverton, OR 97006

Principal Investigator: J. S. Blakemore, Professor
Dep't. of Applied Physics and
Electrical Engineering
Phone: 503-690-1133

Contract Dates: August 29, 1984 - August 28, 1985

Reporting Period: August 29, 1984 - August 28, 1985

Report Submitted by:

J. S. Blakemore
Principal Investigator

R. E. Kremer
Faculty Associate

UNCLASSIFIED
SECURITY CLASSIFICATION OF THIS PAGE

REPORT DOCUMENTATION PAGE

1a. REPORT SECURITY CLASSIFICATION: UNCLASSIFIED	1b. RESTRICTIVE MARKINGS: NONE
2a. SECURITY CLASSIFICATION AUTHORITY	3. DISTRIBUTION/AVAILABILITY OF REPORT: Approved for Public Release Distribution Unlimited
2b. DECLASSIFICATION/DOWNGRADING SCHEDULE	
4. PERFORMING ORGANIZATION REPORT NUMBER(S): 71-521-SA-2	5. MONITORING ORGANIZATION REPORT NUMBER(S)
6a. NAME OF PERFORMING ORGANIZATION: Oregon Graduate Center; 6b. OFFICE SYMBOL (If applicable)	7a. NAME OF MONITORING ORGANIZATION: Office of Naval Research/Seattle
6c. ADDRESS (City, State and ZIP Code): 19600 NW Von Neumann Drive, Beaverton, Oregon 97006-1999	7b. ADDRESS (City, State and ZIP Code): 315 University District Building, 1107 NE 45 Street, Seattle, WA 98105
8a. NAME OF FUNDING/SPONSORING ORGANIZATION: Defense Advanced Projects Research Agency; 8b. OFFICE SYMBOL (If applicable)	9. PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER: MDA903-84-K-0374
8c. ADDRESS (City, State and ZIP Code): 1400 Wilson Boilevard, Arlington, VA 22209	10. SOURCE OF FUNDING NOS.

PROGRAM ELEMENT NO.	PROJECT NO.	TASK NO.	WORK UNIT NO.
ARPA Order 5020/1		Program Code 4D10	

11. TITLE (Include Security Classification): Transient Velocity Assessment in GaAs (Unclassified)

12. PERSONAL AUTHOR(S): J. S. Blakemore and R. E. Kremer

13a. TYPE OF REPORT	13b. TIME COVERED	14. DATE OF REPORT (Yr., Mo., Day)	15. PAGE COUNT
Final Technical	FROM 84/8 TO 85/8	85-10-22	106

16. SUPPLEMENTARY NOTATION: NONE

17 COSATI CODES		
FIELD	GROUP	SUB. GR.

18. SUBJECT TERMS (Continue on reverse if necessary and identify by block number): Gallium arsenide, submicron devices, ballistic transport, velocity saturation, semiconductor substrate evaluation, semi-insulating materials, electron defect evaluation

19. ABSTRACT (Continue on reverse if necessary and identify by block number)

The final report for a 12-month program containing four tasks in two general areas of concern for GaAs device technology. Task I was to assemble and evaluate literature and other databases concerning high speed operation as assisted by velocity overshoot or ballistic transport; a bibliography of 232 items appears with this Report. Task II involved assessment of the probability of achieving ballistic or other maximized electron speed with various sub-micron geometry GaAs devices, and the report here emphasizes the higher probability of eventual success with vertically-oriented devices, especially HBTs. Task III involved literature and other database assessment for EL2 and other extrinsic properties of GaAs; it is noted here that, despite intense study by many, the atomic nature of EL2 is not determined, and that research on the high temperature defect chemistry of GaAs is desirable. Task IV involved mapping measurements of EL2 and other properties of SI GaAs wafers, and the part of our work carried out in support of DARPA needs is described.

20 DISTRIBUTION/AVAILABILITY OF ABSTRACT	21. ABSTRACT SECURITY CLASSIFICATION
UNCLASSIFIED/UNLIMITED ☒ SAME AS RPT. ☐ DTIC USERS ☐	UNCLASSIFIED

22a. NAME OF RESPONSIBLE INDIVIDUAL	22b TELEPHONE NUMBER (Include Area Code)	22c OFFICE SYMBOL
Sven A. Roosild	202-694-3010	DARPA/DSO

DD FORM 1473, 83 APR — EDITION OF 1 JAN 73 IS OBSOLETE.

UNCLASSIFIED
SECURITY CLASSIFICATION OF THIS PAGE

TABLE OF CONTENTS

TRANSIENT VELOCITY ASSESSMENT IN GALLIUM ARSENIDE, AND OF OTHER GaAs CHARACTERISTICS RELATED TO DEVICE FUNCTIONS

Final Technical Report

Executive Summary

Our efforts during this 12-month study have been divided into the areas of four tasks, in two general areas of GaAs technology. These are:

I. Collection and assessment of literature and other database information concerning experimental and theoretical aspects of high electronic velocity phenomena in GaAs.

II. A critique of the above literature, to suggest guidelines for future DARPA-sponsored work on high-speed GaAs device concepts.

III. Collection and assessment of data concerning EL2 and other significant extrinsic properties in semi-insulating (SI) gallium arsenide.

IV. A summary of work that has been done in various laboratories to map properties of GaAs wafers (such as EL2 density), and of comparable attempts to map device parameter shifts across GaAs wafers. This has been complemented by work done at the Oregon Graduate Center for quantitative mapping of EL2 concentration etc., work done partly under NSF sponsorship and partly to provide information assisting DARPA programs.

The data collection involved in Task I was deliberately restricted, in the latter stages of the work, to concentrate on

device concepts having the greatest potential (in our estimation) for achieving significant velocity overshoot or ballistic transport. Our conclusion is that the greatest potential lies with vertically-oriented devices, rather than those (such as normal MESFETs, or MODFETs) with electron transport parallel to the surface. Thus the bibliography of 232 items contained within Part I of this Report has more than half of the entries dealing with vertically oriented geometry concepts and experiments: the permeable base transistor, the planar-doped barrier transistor, the heterojunction bipolar transistor (HBT), and some other even more specialized device concepts.

Part II of the Report reports on our critique and assessment not only of where these devices stand now, but their potential (if any) for substantial further improvement. Comments are made concerning each of the three device arrangements just mentioned above, with the maximum optimism expressed (still with caution) for the HBT. The permeable base transistor's dependence on improved lithography for any improvement in speed is noted as a likely limitation; while the scattering of electrons by coupled plasmon-optical phonon modes appears a severe drawback for planar-doped barrier devices. Difficulties with HBTs <u>are</u> noted, particularly the conduction band spike that will occur at each heterojunction (and a HBT may have heterojunctions at the emitter end alone, or at both ends of the base) unless a regime of compositional and doping grading can be laid down (typically by epitaxy) to avert this problem.

Part III of the report contains a discussion of the large amount of work which has gone on worldwide over the past eight years to elucidate the atomic nature of the midgap defect known generally as EL2. Despite all this work, and despite a strong presumption that a As_{Ga} antisite is involved in EL2, there has been no unanimity of scientific opinion as to whether EL2 could be an isolated antisite (apparently ruled out by some experiments) or whether this is part of a complex involving two (or perhaps even more) sites. It appears to us a matter of importance that this problem should be solved, and that increased attention to the high temperature defect chemistry of GaAs is an essential in doing so.

Understanding of the precise nature of EL2 is important since it is present in a concentration large enough (up to 1 ppma) to control the Fermi energy in undoped GaAs; and since that concentration is affected by the conditions of growth, annealing, etc. In the absence, to date, of that full understanding, it does become particularly important that EL2 concentration, its variation across a wafer and through an ingot, and from one ingot to another, be measured - so that at least some degree of control can be exercised pending full understanding. It is also important to map other significant extrinsic variables of GaAs, and the question arises: which are the most important ones? Dislocations have been examined in several recent studies, though it is not clear whether a dislocation affects a device such as a GaAs MESFET directly, or only indirectly.

In the concluding sections of the narrative reported here,

Part IV of the Report lists papers that have appeared in recent years concerning attempts to map, and to correlate, various extrinsic properties of GaAs (resistivity, dislocations, EL2, carbon, etc.) and device parameters. That list includes work carried out at the Oregon Graduate Center for the mapping of EL2, dislocations, and correlation with resulting properties of devices fabricated at Triquint Semiconductor. A conclusion of that work is that the local EL2 concentration is significant in determining MESFET parameters such as V_{th} and I_{dss}. Part IV of the Report additionally illustrates information about EL2 mapping done in order to assist other DARPA contractors, including measurements made of wafers surface-treated at ARACOR, and EL2 maps for wafers from crystals grown at Westinghouse.

Final Technical Report

We will now discuss the program in detail, dividing the report into the same four areas mentioned in the summary. These tasks are reported on in Parts I through IV of the Report.

I. Collection of literature concerning high electronic velocity in GaAs.

Throughout the year that this report covers, we have been collecting literature dealing with the general topic of high electronic velocity in GaAs and other similar materials. In addition to searching the pre-existing literature, we have been continually adding to our collection from the current literature.

During the first six months of this contract, we concentrated primarily on studying the limitations to electronic velocity in GaAs and related materials. This part of the work dealt with the different scattering mechanisms that influence the mean free path of the carriers, as well as properties of the materials themselves. From this initial study, which will be discussed in Part II of this report, we arrived at the conclusion that devices where the carrier motion is vertically oriented offer the best possibilities to exploit the higher electronic velocities present in GaAs.

The study of various vertically-oriented devices occupied the second half of this project. We collected literature dealing

with a number of different geometries, all of which show considerable promise. The device structures most discussed in the literature are the permeable base transistor, the planar doped barrier transistor and the heterojunction bipolar transistor. We have concentrated primarily on these three device types, although others were also briefly considered.

Our library, then, has been divided into several categories. The first, (Section I.A) deals with general topics from the first period of the study. We then have sub-sections for each of the three main device types considered, as well as a brief listing for other structures. It should be pointed out that we have not included any of the voluminous literature concerning devices where the electronic flow is parallel to the surface, or horizontal. This exclusion eliminates all mention of devices such as standard-geometry FETs, MODFETs or HEMTs, 2DEG, etc. Our library comprises the remainder of Part I.

The bibliographic listings extending over pages 10 through 44 of this Report contain 232 items in all, and are sequentially numbered 1 through 232 in the left margins of these pages. As noted again on page 44, that permits us, in the narrative of Part II of this Report (starting on page 45) to cite any one of these items by its number in parentheses. Thus, a citation (155) directs the reader to the 1982 paper on HBTs by Kroemer listed on page 32.

BIBLIOGRAPHY

Note on the GaAs High Electron Velocity Bibliography

This bibliography is not intended to be complete. It has been divided into two main sections, the first containing papers that discuss ballistic transport, velocity overshoot and similar topics of a general nature. The second section contains literature dealing with specific three-terminal devices, and is further divided into several subsections, each of which deals with a different device geometry. Due to our belief that devices that hope to utilize the high electronic velocity in GaAs and related materials to its highest capabilities must have the electronic motion in a direction perpendicular to the surface of the device, we have not included any of the voluminous literature on surface-parallel geometries such as FETs, HEMTs, MODFETs, etc. The literature is arranged chronologically by year and alphabetically by first author within each year.

I.A. GENERAL BIBLIOGRAPHY

1961

1. B. K. Ridley and T. B. Watkins, "The Possibility of Negative Resistance Effects in Semiconductors," Proc. Phys. Soc.(Lond.) 78, 293 (1961).

1962

2. C. Hilsum, "Transferred Electron Amplifiers and Oscillators," Proc. IRE 50, 185 (1962).

1967

3. J. G. Ruch and G. S. Kino, "Measurement of the Velocity-Field Characteristic of Gallium Arsenide," Appl. Phys. Lett. 10, 40, (1967).

1968

4. E. M. Conwell and M. O. Vassell, "High-Field Transport in n-Type GaAs," Phys. Rev. 166, 797 (1968).

1972

5. J. G. Ruch, "Electron Dynamics in Short Channel Field-Effect Transistors," IEEE Trans. - Elec. Dev. ED-19, 652 (1972).

1975

6. B. W. Clark, H. G. B. Hicks, I. G. A. Davies and J. S. Heeks, "A (GaAl)As - GaAs Heterojunction Structure for Studying the Role of the Cathode Contact on Transferred Electron Devices," Inst. Phys. Conf. Ser. 24, 373 (1975).

7. L. P. Zverev, G. M. Min'kov and N. K. Sumin, "Heating of Electrons in GaAs at Low Temperatures," Sov. Phys. - Semicond. 9, 503 (1975).

1977

8. P. A. Houston and A. G. R. Evans, "Electron Drift Velocity in n-GaAs at High Electric Fields," Solid State Elect. 20, 197 (1977).

9. M. A. Littlejohn, J. R. Hauser and T. H. Glisson, "Velocity-Field Characteristics of GaAs with $\Gamma - L - X$ Conduction-Band Ordering," J. Appl. Phys. 48, 4587 (1977).

10. M. A. Littlejohn, J. R. Hauser and T. H. Glisson, "Velocity-Field Characteristics of $Ga_{1-x} In_x P_{1-y} As_y$ Quaternary Alloys," Appl. Phys. Lett. 30,242 (1977).

11. T. J. Maloney and J. Frey, "Transient and Steady-State Electron Transport Properties of GaAs and InP," J. Appl. Phys. 48, 781 (1977).

12. I. Mojzes, B. Podor and I. Balogh, "On the Temperature Dependence of Peak Electron Velocity and Threshold Field Measured on GaAs Gunn Diodes," Phys. Stat. Sol. (a) 39, K123 (1977).

13. H. Rees, G. S. Sanghera and R. A. Warriner, "Low-Temperature FET for Low-Power High-Speed Logic," Elect. Lett. 13, 156 (1977).

1978

14. C. Hilsum, "Historical Background of Hot Electron Physics (A Look Over the Shoulder)," Solid State Elect. 21, 5 (1978).

15. M. A. Littlejohn, J. R. Hauser, T. H. Glisson, D. K. Ferry and J. W. Harrison, "Alloy Scattering and High Field Transport in Ternary and Quaternary III-V Semiconductors," Solid State Elect. 21, 107 (1978).

16. S. Kratzer and J. Frey, "Transient Velocity Characteristics of Electrons in GaAs with Γ^{C}_{6}-L^{C}_{6}-X^{C}_{6} Conduction Band Ordering," J. Appl. Phys. 49, 4064 (1978).

17. H. Kroemer, "Hot-Electron Relaxation Effects in Devices," Solid State Elect. 21, 61 (1978).

18. P. J. Price, "Calculation of Hot Electron Phenomena," Solid State Elect. 21, 9 (1978).

1979

19. J. R. Hauser, T. H. Glisson and M. A. Littlejohn, "Negative Resistance and Peak Velocity in the Central (000) Valley of III-V Semiconductors," Solid State Elect. 22, 487 (1979).

20. M. A. Littlejohn, L. A. Arledge, T. H. Glisson and J. R. Hauser, "Influence of Central Valley Effective Mass and Alloy Scattering on Transient Drift Velocity in $Ga_{1-x}In_{x}P_{1-y}As_{y}$," Elect. Lett. 15, 586 (1979).

21. M. S. Shur and L. F. Eastman, "Ballistic Transport in Semiconductor at Low Temperatures for Low-Power High-Speed Logic," IEEE Trans. - Elec. Dev. ED-26, 1677 (1979).

22. T. Wada and J. Frey, "Physical Basis of Short-Channel MESFET Operation," IEEE Jour. Solid-State Cir. SC-14, 398 (1979).

1980

23. J. R. Barker, D. K. Ferry and H. L. Grubin, "On the Nature of Ballistic Transport in Short-Channel Semiconductor Devices," IEEE Elec. Dev. Lett. EDL-1, 209 (1980).

24. J. R. Barker and D. K. Ferry, "On the Physics and Modeling of Small Semiconductor Devices," Solid State Elect. 23, 519, 531, and 545 (1980).

25. B. Carnez, A. Cappy, A. Kaszynski, E. Constant and G. Salmer, "Modeling of a Submicrometer Gate Field-Effect Transistor including Effects of Nonstationary Electron Dynamics," J. Appl. Phys. 51, 784 (1980).

26. L. F. Eastman, R. Stall, D. Woodard, N. Dandekar, C. E. C. Wood, M. S. Shur, and K. Board, "Ballistic Electron Motion in GaAs at Room Temperature," Elect. Lett. 16, 524 (1980).

27. W. R. Frensley, "High-Frequency Effects of Ballistic Electron Transport in Semiconductors," IEEE Elec. Dev. Lett. EDL-1, 137 (1980).

28. J. Frey, "Ballistic Transport in Semiconductor Devices," IEDM - 1980, p. 613.

29. K. Kamei, S. Hori, H Kawasaki, T. Chigira and K Kawabuchi, "Quarter Micron Gate Low Noise GaAs FETs Operable up to 30 GHz," IEDM -1980, p. 102.

30. T. J. Maloney, "Polar Mode Scattering in Ballistic Transport GaAs Devices," IEEE Elec. Dev. Lett. EDL-1, 54 (1980).

31. J. Pozela and A. Reklaitis, "Electron Transport Properties in GaAs at High Electric Fields," Solid State Elect. 23, 927 (1980).

32. H. Shichijo, "Theoretical Studies of High Field Transport in III-V Semiconductors," Ph.D. Thesis, University of Illinois, 1980.

33. H. Shichijo, K. Hess and G. E. Stillman, "Orientation Dependence of Ballistic Electron Transport and Impact Ionisation," Elect. Lett. 16, 208 (1980).

34. M. S. Shur and L. F. Eastman, "GaAs n^+ -p^- -n^+ Ballistic Structure," Elect. Lett. 16, 522 (1980).

35. M. S. Shur and L. F. Eastman, "Ballistic and Near Ballistic Transport in GaAs," IEEE Elec. Dev. Lett. EDL-1, 147 (1980).

36. P. M. Smith, M. Inoue and J. Frey, "Electron Velocity in Si and GaAs at Very High Electric Fields," Appl. Phys. Lett. 37, 797 (1980).

37. J. B. Socha and G. J. Rees, "Ballistic Electron Transport in a Nonparabolic Band," Elect. Lett. 16, 872 (1980).

1981

38. F. Capasso, T. P. Pearsall and K. K. Thornber, "The Effect of Collisional Broadening on Monte Carlo Simulations of High-Field Transport in Semiconductor Devices," IEEE Elec. Dev. Lett. EDL-2, 295 (1981).

39. R. K. Cook and J. Frey, "Diffusion Effects and 'Ballistic Transport,'" IEEE Trans. - Elec. Dev. ED-28, 951 (1981).

40. W. R. Curtice and Y-H. Yun, "A Temperature Model for the GaAs MESFET," IEEE Trans. - Elec. Dev. ED-28, 954 (1981).

41. J. Degani, R. F. Leheny, R. E. Nahory and J. P. Heritage, "Velocity Field Characteristics of Minority Carriers (Electrons) in p-In_x Ga_y As," Appl. Phys. Lett. 39, 569 (1981).

42. L. F. Eastman, R. Stall, D. Woodard, C. E. C. Wood, N. Dandekar, M. Shur, M. Hollis and K. Board, "Ballistic Electron Transport in Thin Layers of GaAs," Inst. Phys. Conf. Ser. 56, 185 (1981).

43. D. K. Ferry, J. Zimmermann, P. Lugli and H. Grubin, "Limitations to Ballistic Transport in Semiconductors," IEEE Elec. Dev. Lett. EDL-2, 228 (1981).

44. K. Hess, "Comment on 'Effect of Collisional Broadening on Monte Carlo Simulations of High-Field Transport in Semiconductor Devices,'" IEEE Elec. Dev. Lett. EDL-2, 297 (1981).

45. K. Hess, "Ballistic Electron Transport in Semiconductors," IEEE Trans. - Elec. Dev. ED-28, 937 (1981).

46. A. A. Kastalsky and M. S. Shur, "Conductance of Small Semiconductor Devices," Solid State Comm. 39, 715 (1981).

47. S. Laval, C. Bru, R. Castagne and C. Arnodo, "Experimental Evidence for Velocity Overshoot in AsGa from Photoconduction Measurements," Inst. Phys. Conf. Ser. 56, 171 (1981).

48. J. Lee, " The Probability for Ballistic Electron Motion in n-GaAs," IEEE Elec. Dev. Lett. EDL-2, 167 (1981).

49. J. Lee, "Ballistic Transport in a Nonparabolic Band Structure," J. Appl. Phys. 52, 4676 (1981).

50. J. P. Nougier, J. C. Vaissiere, D. Gasquet, J. Zimmermann and E. Constant, "Determination of Transient Regime of Hot Carriers in Semiconductors, Using the Relaxation Time Approximations," J. Appl. Phys. 52, 825 (1981).

51. P. E. Schmidt, M. Octavio and P. D. Esqueda, "Single-Carrier Space-Charge Controlled Conduction vs. Ballistic Transport in GaAs Devices at 77 K," IEEE Elec. Dev. Lett. EDL-2, 205 (1981).

52. C. V. Shank, R. L. Fork, B. I. Greene, F. K. Reinhart and R. A. Logan, "Picosecond Nonequilibrium Carrier Transport in GaAs," Appl. Phys. Lett. 38, 104 (1981).

53. H. Shichijo and K. Hess, "Band-Structure-Dependent Transport and Impact Ionization in GaAs," Phys. Rev. B 23, 4197 (1891).

54. M. S. Shur and L. F. Eastman, "Near Ballistic Electron Transport in GaAs Devices at 77 K," Solid State Elect. 24, 11 (1981).

55. M. S. Shur, "Ballistic Transport in a Semiconductor with Collisions," IEEE Trans. - Elec. Dev. ED-28, 1120 (1981).

1982

56. Y. Awano, K. Tomizawa, N. Hashizume and M. Kawashima, "Compensation Tendency of Short-Channel and Narrow-Channel Effects in Small-Geometry IGFETs," Elect. Lett. 18,133, (1982).

57. R. K. Cook and J. Frey, "Two-Dimensional Numerical Simulation of Energy Transport Effects in Si and GaAs MESFETs," IEEE Trans. - Elec. Dev. ED-29, 970 (1892).

58. L. F. Eastman, "The Limits of Electron Ballistic Motion in Compound Semiconductor Transistors," Inst. Phys. Conf. Ser. 63, 245 (1982).

59. R. C. Eden, "Comparison of GaAs Device Approaches for Ultrahigh-Speed VLSI," Proc. IEEE 70, 5 (1982).

60. R. C. Eden and B. M. Welch, "Ultra-High-Speed GaAs VLSI: Approaches, Potential and Progress," VLSI Electronics 3, 109 (1982).

61. J. V. Faricelli, J. Frey and J. P. Krusius, "Physical Basis of Short-Channel MESFET Operation II: Transient Behavior," IEEE Trans. - Elec. Dev. ED-29, 377 (1982).

62. T. H. Glisson, C. K. Williams, J. R. Hauser and M. A. Littlejohn, "Transient Response of Electron Transport in GaAs Using the Monte Carlo Method," VLSI Electronics 4, 99 (1982).

63. R. O. Grondin, P. Lugli and D. K. Ferry, "Ballistic Transport in Semiconductors," IEEE Elec. Dev. Lett. EDL-3, 373 (1982).

64. J. A. Higgins and D. N. Pattanayak, "A Numerical Approach to Modeling the Ultrashort-Gate MESFET," IEEE Trans. - Elec. Dev. ED-29, 179 (1982).

65. A. J. Holden and B. T. Debney, "Improved Theory of Ballistic Transport in One Dimension," Elect. Lett. 18 558 (1982).

66. S. E. Kumekov and V. I. Perel', "Relaxation of Fast Electrons in Semiconductors at Coupled Plasmon-Phonon Oscillations," Sov. Phys. - Semicond. 16, 1291 (1982).

67. J. Lee and C. B. Su, "Near Ballistic Transport in a Nonparabolic-Band Structure for n- and p-GaAs," IEEE Trans. - Elec. Dev. ED-29, 933 (1982).

68. J.-F. Pone, R. C. Castagne, J.-P. Courat and C. Arnodo, "Two-Dimensional Particle Modeling of Submicrometer Gate GaAs FETs Near Pinchoff," IEEE Trans. - Elec. Dev. ED-29, 1244 (1982).

69. J. B. Socha and L. F. Eastman, "Comment on 'Single-Carrier Space-Charge Controlled Conduction vs. Ballistic Transport in GaAs Devices at 77 K,'" IEEE Elec. Dev. Lett. EDL-3, 27 (1982).

70. J. Y-F. Tang and K. Hess, "Investigation of Transient Electronic Transport in GaAs Following High Energy Injection," IEEE Trans. - Elec. Dev. ED-29, 1906 (1982).

71. K. K. Thornber, "Current Equations for Velocity Overshoot," IEEE Elec. Dev. Lett. EDL-3, 69, (1982).

1983

72. A. Aishima and Y. Fukushima, "New Negative Conductance in GaAs n^+-n-n^+ Ballistic Diode -- Time-Dependent Computer Simulation," Jap. J. Appl. Phys. 22, 1889 (1983),

73. S. J. Allen, Jr., C. L. Allyn, H. M. Cox, F. DeRosa and G. E. Mahoney, "Dispersion of the Saturated Current in GaAs from dc to 1200 GHz," Appl. Phys. Lett. 42, 96 (1983).

74. Y. Awano, K. Tomizawa, N. Hashizume and M. Kawashima, "Monte Carlo Particle Simulation of a GaAs Short-Channel MESFET," Elect. Lett. 19, 20 (1983).

75. K. Brennan, K. Hess and G. J. Iafrate, "Monte Carlo Simulation of Reflecting Contact Behavior on Ballistic Device Speed," IEEE Elec. Dev. Lett. EDL-4, 332 (1983).

76. F. A. Buot and J. Frey, "Effects of Velocity Overshoot on Performance of GaAs Devices with Design Information," Solid State Elect. 26, 617 (1983).

77. A. Ghis, E. Constant and B. Boittiaux, "Ballistic and Overshoot Electron Transport in Bulk Semiconductors and in Submicronic Devices," J. Appl. Phys. 54, 214 (1983).

78. R. K. Mains, G. I. Haddad and P. A. Blakey, "Simulation of GaAs IMPATT Diodes Including Energy and Transport Equations," IEEE Trans. - Elec. Dev. ED-30, 1327 (1983).

79. G. Y. Robinson and M. S. Shur, "Electron Ballistic Effects in III-V Semiconductors," Final Report to ARO, 1983.

80. N. Sawaki, "Non-Linear Transport and Transient Properties of Semiconductors Under High Electric Field," J. Phys. C 16, 4611 (1983).

81. A. A. Sukhanov, V. B. Sandomirskii and Yu. Ya. Tkach, "Theory of Static Current-Voltage Characteristics of Ballistic Metal-Insulator-Semiconductor Transistors," Sov. Phys. - Semicond. 17, 1378 (1983).

82. C. L. Tang and D. J. Erskine, "Femtosecond Relaxation of Photoexcited Nonequilibrium Carriers in $Al_x Ga_{1-x} As$," Phys. Rev. Lett. 51, 840 (1983).

83. A. van der Ziel, M. S. Shur, K. Lee, T-H. Chen and K. Amberiadis, "Carrier Distribution and Low-Field Resistance in Short n^+-n^--n^+ and n^+-p^--n^+ Structures," IEEE Trans. - Elec. Dev. ED-30, 128 (1983).

84. A. R. Vasconcellos and R. Luzzi, "Ultrafast Transient Transport in Nonequilibrium Semiconductors," Phys. Rev. B 27, 3874 (1983).

85. C. K. Williams, T. H. Glisson, M. A. Littlejohn and J. R. Hauser, "Ballistic Transport in GaAs," IEEE Elec. Dev. Lett. EDL-4, 161 (1983).

1984

86. Y. Awano, K. Tomizawa and N. Hishizume, "Principles of Operation of Short-Channel Gallium Arsenide Field-Effect Transistor Determined by Monte Carlo Method," IEEE Trans. - Elec. Dev. ED-31, 448 (1984).

87. K. Brennan and K. Hess, "High Field Transport in GaAs, InP and InAs," Solid State Elect. 27, 347 (1984).

88. K. Brennan, K. Hess and G. J. Iafrate, "Monte Carlo Investigation of Transient Hole Transport in GaAs," J. Appl. Phys. 55, 3632 (1984).

89. A. Ghosal, D. Chattopadhyay and N. N. Purkait, "Hot-Electron Velocity Overshoot in $Ga_{.47}$ $In_{.53}$ As," Appl. Phys. Lett. 44, 773 (1984).

90. R. O. Grondin, P. A. Blakey and J. R. East, "Effects of Transient Carrier Transport in Millimeter-Wave GaAs Diodes," IEEE Trans. - Elec. Dev. ED-31, 21 (1984).

91. H. L. Grubin, K. Hess, G. J. Iafrate and D. K. Ferry (ed.), "The Physics of Submicron Structures," Plenum Press, 1984.

92. A. A. Ignatov and A. V. Okomelkov, "Comments on the Nature of Ballistic Transport in Small Semiconductor Devices at Low Applied Voltage," Solid State Comm. 50, 677 (1984).

93. J. S. Moore and P. Das, "Hot Carrier Transient Response in Bulk III-V Compounds," J. Appl. Phys. 56, 375 (1984).

94. T. Mori, C. Hamaguchi, A. Shibatomi and O. Ryuzan, "Hot Electron Effect in Short n^+nn^+ GaAs," Jap. J. Appl. Phys. 23, 212 (1984).

95. V. I. Ryzhii, N. A. Bannov and V. A. Fedirko, "Ballistic and Quasiballistic Transport in Semiconductor Structures (Review)," Sov. Phys. - Semicond. 18, 481 (1984).

1985

96. J. R. Barker, M. Mudares, B. R. Snell, P. S. S. Guimaraes, D. C. Taylor, L. Eaves and G. Hill, "Validation of Magnetophonon Spectroscopy as a Tool for Analyzing Hot-Electron Effects in Devices," Appl. Phys. Lett. 47, 387 (1985).

97. M. H. Evanno, B. Boittiaux, A. Safrioui and R. Fauquembergue, "Experimental Determination of Velocity-Field Characteristic in N-GaAs and n-GaInAs/InP Using a New Method Based on the Magnetoresistance Effect," Inst. Phys. Conf. Ser. 74, 229 (1985).

98. Y-K. Feng, "New v(E) Relationship for GaAs," Elect. Lett. 21, 453 (1985).

99. H. L. Grubin, J. P. Kreskovsky, M. Meyyappan and B. J. Morrison, "Semiconductor Materials for High Frequency Solid State Sources," Final report to DARPA, 1985.

100. P. Hesto, C. Bru, S. Laval and R. Castagne, "Quasiballistic Transport in GaAs at 77 K: A Comparison Between Monte-Carlo Simulations and Photoconductivity Measurements in Submicron Structures," Inst. Phys. Conf. Ser. 74, 635 (1985).

101. R. A. Hopfel, J. Shah, A. C. Gossard and W. Weigmann, "Hot Carrier Drift Velocities in GaAs / AlGaAs Multiple Quantum Well Structures," Proc. 4th Int. Conf. on Hot Electrons in Semicond., Innsbruck, 1985, in press.

102. R. H. Johnson and O. Eknoyan, "High-Field Electron Drift Velocity Measurements in Gallium Phosphide," J. Appl. Phys. 58, 1402 (1985).

103. D. Lowe and J. R. Barker, "A Model Study of Field-Dependent Dynamical Screening Due to Mobile Electrons in Submicron Semiconductor Devices," J. Phys. C 18, 2507 (1985).

104. K. Matsumoto, N. Hashizume, N. Atoda and Y. Awano, "Effects of p-type Barrier Layer on Characteristics of Sub-Micron Gate Self-Aligned GaAs FET," Inst. Phys. Conf. Ser. 74, 515 (1985).

105. T. Ohashi, M. I. Nathan, S. D. Mukherjee, G. W. Wicks, G. Rubino and L. F. Eastman, "Electron Velocity vs Electric Field in n-type $Ga_{1-x}In_x$ As Short Samples -- Evidence for Ballistic Transport," Inst. Phys. Conf. Ser. 74, 293 (1985).

106. K. Tsubaki, T. Fukai and H. Saito, "High Field Electron Transport in n-InP / GaInAs Two-Dimensional Electron Gas," Appl. Phys. Lett. 46, 875 (1985).

I.B. PERMEABLE BASE TRANSISTOR BIBLIOGRAPHY

1980

107. G. D. Alley, C. O. Bozler, D. C. Flanders, R. A. Murphy and W. T. Lindley, "Recent Experimental Results on Permeable Base Transistors," IEDM - 1980, p. 608.

108. C. O. Bozler and G. D. Alley, "Fabrication and Numerical Simulation of the Permeable Base Transistor," IEEE Trans. - Elec. Dev. ED-27, 1128 (1980).

1982

109. G. D. Alley, C. O. Bozler, N. P. Economou, D. C. Flanders, M. W. Geis, G. A. Lincoln, W. T. Lindley, R. W. McClelland, R. A. Murphy, K. B. Nichols, W. J. Piacentini, S. Rabe, J. P. Salerno and B. A. Vojak, "Millimeter-Wavelength GaAs Permeable Base Transistors," IEEE Trans. - Elec. Dev. ED-29, 1708 (1982).

110. C. O. Bozler and G. D. Alley, "The Permeable Base Transistor and Its Applications to Logic Circuits," Proc. IEEE 70, 46 (1982).

111. U. Mishra, E. Kohn, N. J. Kawai and L. F. Eastman, "Permeable Base Transistor - A New Technology," IEEE Trans. - Elec. Dev. ED-29, 1707 (1982).

1983

112. W. R. Frensley, "Barrier-Limited Transport in Semiconductor Devices," IEEE Trans. - Elec. Dev. ED-30, 1619 (1983).

113. W. R. Frensley, "An Analytic Model for the Barrier-Limited Mode of Operation of the Permeable Base Transistor," IEEE Trans. - Elec. Dev. ED-30, 1624 (1983).

114. M. A. Osman, D. H. Navon, T-W. Tang and L. Sha, "Improved Design of the Gallium Arsenide Permeable Base Transistor," IEEE Trans. - Elec. Dev. ED-30, 1348 (1983).

115. B. A. Vojak, J. P. Salerno, D. C. Flanders, G. D. Alley, C. O. Bozler, K. B. Nichols, R. W. McClelland, N. P. Economou, G. A. Lincoln, R. A. Murphy, W. T. Lindley and G. D. Johnson, "Transmission Electron Microscopy of GaAs Permeable Base Transistor Grown by Vapor Phase Epitaxy," J. Appl. Phys. 54, 3554 (1983).

1984

116. H. Asai, S. Adachi, S. Ando and K. Oe, "Lateral GaAs Growth Over Tungsten Gratings on (001) GaAs Substrates by Metalorganic Chemical Vapor Deposition and Applications to Vertical Field-Effect Transistors," J. Appl. Phys. 55, 3868 (1984).

117. J. L. Rienstra, "Electron Traps in the GaAs Permeable Base Transistor," M. S. Thesis, Mass. Inst. Tech., 1984.

118. B. A. Vojak, R. W. McClelland, G. A. Lincoln, A. R. Calawa, D. C. Flanders and M. W. Geis, "A Self-Alligned Dual-Grating GaAs Permeable Base Transistor," IEEE Elec. Dev. Lett. EDL-5, 270 (1984).

119. X. C. Zhu, X. N. Zhang, A. van der Ziel and C. O. Bozler, "Low-Frequency Noise in Permeable Base Transistors," IEEE Trans - Elec. Dev. ED-31, 1408 (1984).

1985

120. S. Adachi, S. Ando, H. Asai and N. Susa, "A New Gate Structure Vertical-GaAs FET," IEEE Elec. Dev. Lett. EDL-6, 264 (1985).

121. H. Asai and S. Ando, "Lateral Growth Process of GaAs over Tungsten Gratings by Metalorganic Chemical Vapor Deposition," J. Electrochem. Soc. 132, 2445 (1985).

122. Y. Awano, K. Tomizawa and N. Hashizume, "Electrical Performances of GaAs Permeable Base Ballistic Electron Transistors," Inst. Phys. Conf. Ser. 74, 623 (1985).

123. C-G. Hwang, D. H. Navon and T-W. Tang, "Nonstatic Effects in the GaAs Permeable Base Transistor," IEEE Elec. Dev. Lett. EDL-6, 114 (1985).

124. N. Kondo, M. Kawashima, S. Ando and K. De, "GaAs Lateral Epitaxial Growth Over a Tungsten Grating by Molecular Beam Epitaxy," Appl. Phys. Lett. 46, 436 (1985).

I.C. PLANAR-DOPED BARRIER TRANSISTOR BIBLIOGRAPHY

1980

125. R. J. Malik, K. Board, L. F. Eastman, C. E. C. Wood, T. R. AuCoin, R. L. Ross, and R. O. Savage, "GaAs Planar Doped Barriers by Molecular Beam Epitaxy," IEDM - 1980, p.456 (1980).

1981

126. R. F. Kazarinov and S. Luryi, "Charge Injection Over Triangular Barriers in Unipolar Semiconductor Structures," Appl. Phys. Lett. 38, 810 (1981).

1982

127. J. A. Barnard, R. E. Najjar, S. C. Palmateer, M. Hollis and L. F. Eastman, "High Responsivity Homojunction GaAs Triangular Barrier Photodiode," IEEE Trans. - Elec. Dev, ED-29, 1668 (1982).

128. A. Chandra and L. F. Eastman, "Quantum Mechanical Reflection at Triangular 'Planar-Dpoed' Potential Barriers for Transistors," J. Appl. Phys. 53, 9165 (1982).

129. R. J. Malik and S. Dixon, "GaAs Subharmonically-Pumped Planar Doped Barrier Mixer Diodes," IEEE Trans. - Elec. Dev. ED-29, 1710 (1982).

1983

130. R. K. Cook, "Computer Simulation of Carrier Transport in Planar Doped Barrier Diodes," Appl. Phys. Lett. 42, 439 (1983).

131. M. A. Hollis, S. C. Palmateer, L. F. Eastman, N. V. Dandekar and P. M. Smith, "Importance of Electron Scattering with Coupled Plasmon-Optical Phonon Modes in GaAs Planar-Doped Barrier Transistors," IEEE Elec. Dev. Lett. EDL-4, 440 (1983).

132. G. J. Iafrate, R. J. Malik, J. Y. Tang and K. Hess, "Transient Transport and Transferred Electron Behavior in Gallium Arsenide Under the Condition of High-Energy Electron Injection," Solid State Comm. 45, 255 (1983).

133. M. A. Littlejohn, R. J. Trew, J. R. Hauser and J. M. Golio, "Electron Transport in Planar-Doped Barrier Structures Using an Ensemble Monte Carlo Method," J. Vac. Sci. Tech. B 1, 449 (1983).

1984

134. J. R. Hayes, A. F. J. Levi and W. Wiegmann, "Hot Electron Spectroscopy," Elect. Lett. 20, 851 (1984).

135. S. Luryi, A. Kastalsky, A. C. Gossard and R. H. Hendel, "Charge Injection Transistor Based on Real-Space Hot-Electron Transfer," IEEE Trans. - Elec. Dev. ED-31, 832 (1984).

1985

136. J. R. Hayes, A. F. J. Levi and W. Wiegmann, "Hot Electron Spectroscopy of GaAs," Phys. Rev. Lett. 54, 1570 (1985).

137. P. Lugli and D. K. Ferry, "Investigation of Plasmon-Induced Losses in Quasi-Ballistic Transport," IEEE Elec. Dev. Lett. EDL-6, 25 (1985).

138. S. Luryi, "An Induced Base Hot-Electron Transistor," IEEE Elec. Dev. Lett. EDL-6, 178 (1985).

139. S. Muto, K. Inamura, N. Yokoyama, S. Hiyamizu and H. Nishi, "Subpicosecond Base Transit Time Observed in a Hot-Electron Transistor (HET)," Elect. Lett. 21, 555 (1985).

140. H. Ohnishi, N. Yokoyama and H. Nishi, "Monte Carlo Simulation of Electron Transport Efficiency of an InGaAs/InP Hot-Electron Transistor," IEEE Elec. Dev. Lett. EDL-6, 403 (1985).

141. T. Wang, K. Hess and G. J. Iafrate, "Time-Dependent Ensemble Monte Carlo Simulation for Planar-Doped GaAs Structures," J. Appl. Phys. 58, 857 (1985).

I.D. HETEROJUNCTION BIPOLAR TRANSISTOR BIBLOIGRAPHY

1972

142. W. P. Dumke, J. M. Woodall and V. L. Rideout, "GaAs - GaAlAs Heterojunction Transistor for High Frequency Operation," Solid State Elect. 15, 1339 (1972).

1975

143. M. Konagai and K. Takahashi, "(GaAl)As - GaAs Heterojunction Transistors with High Injection Efficiency," J. Appl. Phys. 46, 2120 (1975).

1977

144. M. Konagai, K. Katsukawa and K. Takahashi, "(GaAl)As / GaAs Heterojunction Phototransistors with High Current Gain," J. Appl. Phys. 48, 4389 (1977).

1979

145. A. Marty, G. Rey and J. P. Bailbe, "Electrical Behavior of an NPN GaAlAs / GaAs Heterojunction Transistor," Solid State Elect. 22, 549 (1979).

1980

146. D. Ankri and A. Scavennec, "Design and Evaluation of a Planar GaAlAs - GaAs Bipolar Transistor," Elect. Lett. 16, 41 (1980).

147. J-P. Bailbe, A. Marty, P. H. Hiep and G. E. Rey, "Design and Fabrication of High-Speed GaAlAs / GaAs Heterojunction Transistors," IEEE Trans. - Elec. Dev. ED-27, 1160 (1980).

148. J. Katz, N. Bar-Chaim, P. C. Chen, S. Margalit, I. Ury, D. Wilt, M. Yust and A. Yariv, "A Monolithic Integration of GaAs / GaAlAs Bipolar Transistor and Heterostructure Laser," Appl. Phys. Lett. 37, 211 (1980).

1981

149. H. Beneking and L. M. Su, "GaAlAs / GaAs Heterojunction Microwave Bipolar Transistor," Elect. Lett. 17, 301 (1981).

1982

150. D. Ankri and L. F. Eastman, "GaAlAs - GaAs Ballistic Heterojunction Bipolar Transistor," Elect. Lett. 18, 750 (1982).

151. P. M. Asbeck, D. L. Miller, W. C. Petersen and C. G. Kirkpatrick, "GaAs / GaAlAs Heterojunction Bipolar Transistors with Cutoff Frequencies Above 10 GHz," IEEE Elec. Dev. Lett. EDL-3, 366 (1982).

152. P. M. Asbeck, D. L. Miller, W. C. Petersen and C. G. Kirkpatrick, "(Ga,Al)As / GaAs Heterojunction Bipolar Transistors: Design Considerations and Experimental Results," IEEE Trans. - Elec. Dev. ED-29, 1706 (1982).

153. C. Y. Chen, A. Y. Cho, P. A. Garbinski and C. G. Bethea, "GaAs / $Al_x Ga_{1-x} As$ Depletion Stop Phototransistor Grown by Molecular Beam Epitaxy," Appl. Phys. Lett. 40, 510 (1982).

154. H. Krautle, P. Narozny and H. Beneking, "Lateral pnp GaAs Bipolar Transistor with Minimized Substrate Currents," IEEE Trans. - Elec. Dev. ED-29, 1707 (1982).

155. H. Kroemer, "Heterostructure Bipolar Transistors and Integrated Circuits," Proc. IEEE 70, 13 (1982).

1983

156. D. Ankri, W. J. Schaff, P. Smith and L. F. Eastman, "High-Speed GaAlAs - GaAs Heterojunction Bipolar Transistors with Near-Ballistic Operation," Elect. Lett. 19, 147 (1983).

157. P. M. Asbeck, D. L. Miller, E. J. Babcock and C. G. Kirkpatrick, "Application of Thermal Pulse Annealing to Ion-Implanted GaAlAs / GaAs Heterojunction Bipolar Transistors," IEEE Elec. Dev. Lett. EDL-4, 81 (1983).

158. F. Capasso, W. T. Tsang, C. G. Bethea, A. L. Hutchinson and B. F. Levine, "New Graded Band-Gap Picosecond Phototransistor," Appl. Phys. Lett. 42, 93 (1983).

159. J. R. Hayes, F. Capasso, A. C. Gossard, R. J. Malik, and W. Wiegmann, " Bipolar Transistor with Graded Band-Gap Base," Elect. Lett. 19, 410 (1983).

160. E. Kohn, U. Mishra and L. F. Eastman, "Short-Channel Effects in 0.5 μm Source-Drain Spaced Vertical GaAs FETs - A First Experimental Investigation," IEEE Elec. Dev. Lett. EDL-4, 125 (1983).

161. R. J. Malik, J. R. Hayes, F. Capasso, K. Alave, and A. Y. Cho, "High-Gain $Al_{0.48}In_{0.52}As/Ga_{0.47}In_{0.53}As$ Vertical n-p-n Heterojunction Bipolar Transistors Grown by Molecular-Beam Epitaxy," IEEE Elec. Dev. Lett. EDL-4, 383 (1983).

162. D. L. Miller, P. M. Asbeck, R. J. Anderson and I. H. Eisen, "(GaAl)As / GaAs Heterojunction Bipolar Transistors with Graded Composition in the Base," Elect. Lett. 19, 367 (1983).

163. S. L. Su, O. Tejayadi, T. J. Drummond, R. Fischer and H. Morkoc, "Double Heterojunction $Al_x Ga_{1-x} As$ / GaAs Bipolar Transistors (DHBJTs) by MBE with a Current Gain of 1650," IEEE Elec. Dev. Lett. EDL-4, 130 (1983).

1984

164. P. M. Asbeck, A. K. Gupta, F. J. Ryan, D. L. Miller, R. J. Anderson, C. A. Liechti and F. H. Eisen, "Microwave Performance of GaAs / (Ga,Al)As Heterojunction Bipolar Transistors," IEDM - 1984, p. 864.

165. P. M. Asbeck, D. L. Miller, R. J. Anderson and F. H. Eisen, "GaAs / (Ga,Al)As Heterojunction Bipolar Transistors with Buried Oxygen-Implanted Isolation Layers," IEEE Elec. Dev. Lett. EDL-5, 310 (1984).

166. P. M. Asbeck, D. L. Miller, R. J. Anderson, L. D. Hou, R. Deming and F. Eisen, "Nonthreshold Logic Ring Oscillators Implemented with GaAs / (Ga,Al)As Heterojunction Bipolar Transistors," IEEE Elec. Dev. Lett. EDL-5, 181 (1984).

167. J. P. Bailbe, A. Marty and G. Rey, "Influence of Degeneracy on Behaviour of Homojunction GaAs Bipolar Transistor," Elect. Lett. 20, 258 (1984).

168. F. Capasso, "Band-Gap Engineering Via Superlattice and Graded-Gap Materials: New Phenomena and Their Device Applications," Proc. 17th Int. Conf. Phys. Semicond., San Francisco, 1984, p. 1537.

169. N. Chand, R. Fischer, T. Henderson, J. Klem, W. Kopp and H. Morkoc, "Temperature Dependence of Current Gain in AlGaAs / GaAs Heterojunction Bipolar Transistors," Appl. Phys. Lett. 45, 1086 (1984).

170. L. C. Chiu, Ch. Harder, S. Margalit and A. Yariv, "Graded Collector Heterojunction Bipolar Transistor," Appl. Phys. Lett. 44, 105 (1984).

171. L. C. Chiu and C. K. Kao, "Application of Abrupt and Graded Gap Structure in High Speed Semiconductor Devices," Jap. J. Appl. Phys. 23, L201 (1984).

172. H. Dambkes, U. Konig and B. Schwaderer, "InGaAs / InP Heterobipolar Transistors for Integration on Semi-Insulating InP Substrates," Elect. Lett. 20, 955 (1984).

173. C. G. Fonstad, "Consideration of the Relative Frequency Performance Potential of Inverted Heterojunction n-p-n Transistors," IEEE Elec. Dev. Lett. EDL-5, 99 (1984).

174. J. R. Hayes, A. C. Gossard and W. Wiegmann, "Collector/Emitter Offset Voltage in Double-Heterojunction Bipolar Transistors," Elect. Lett. 20, 766 (1984).

175. J. R. Hayes, R. F. Leheny, H. Temkin, A. C. Gossard and W. Wiegmann, "Electroluminescence from a Heterojunction Bipolar Transistor," Appl. Phys. Lett. 45, 537 (1984).

176. H. Ito, T. Ishibashi and T. Sugeta, "Extremely Low Resistance Ohmic Contacts to n-GaAs for AlGaAs / GaAs Heterojunction Bipolar Transistors," Jap. J. Appl. Phys. 23, L635 (1984).

177. H. Ito, T. Ishibashi and T. Sugeta, "High-Frequency Characteristics of AlGaAs / GaAs Heterojunction Bipolar Transistors," IEEE Elec. Dev. Lett. EDL-5, 214 (1984).

178. H. Kanbe, J. C. Vlcek and C. G. Fonstad, "(In,Ga)As / InP n-p-n Heterojunction Bipolar Transistors Grown by Liquid Phase Epitaxy with High DC Current Gain," IEEE Elec. Dev. Lett. EDL-5, 172 (1984).

179. S. Kofol, N. Moll, E. Gowen and J. Miller, "GaAs / AlGaAs Heterojunction Bipolar Transistors with Very Low Base Sheet Resistance," IEDM - 1984, p. 198.

180. M. Kurata, and J. Yoshida, "Modeling and Characterization for High-Speed GaAlAs - GaAs n-p-n Heterojunction Bipolar Transistors," IEEE Trans. - Elec. Dev. ED-31, 467 (1984).

181. S-C. Lee, J-N. Kau and H-H. Lin, "Origin of High Offset Voltage in an AlGaAs / GaAs Heterojunction Bipolar Transistor," Appl. Phys. Lett. 45, 1114 (1984).

182. A. N. M. Masum Choudhury, K. Tabatabaie-Alavi and C. G. Fonstad, "Triple Implant (In,Ga)As / InP n-p-n Heterojunction Bipolar Transistors for Integrated Circuit Applications," IEEE Elec. Dev. Lett. EDL-5, 251 (1984).

183. T. Matsuyu, S. Fujita and A. Sasaki, "InGaAsP / InP Wavelength-Selective Heterojunction Phototransistors," IEEE Trans. - Elec. Dev. ED-31, 812 (1984).

184. K. Tomizawa, Y. Awano and N. Hashizume, "Monte Carlo Simulation of AlGaAs / GaAs Heterojunction Bipolar Transistors," IEEE Elec. Dev. Lett. EDL-5, 362 (1984).

185. K. Yokoyama, M. Tomizawa and A. Yoshii, "Accurate Modeling of AlGaAs / GaAs Heterostructure Bipolar Transistors by Two-Dimensional Computer Simulation," IEEE Trans. - Elec. Dev. ED-31, 1222 (1984).

186. N. Yokoyama, K. Imamura, T. Ohshima, H. Nishi, S. Muto, K. Kondo and S. Hiyamizu, "Characterization of Double Heterojunction GaAs / AlGaAs Hot Electron Transistors," IEDM - 1984, p. 532.

187. X. N. Zhang, A. van der Ziel, K. H. Duh and H. Morkoc, "Burst and Low-Frequency Generation-Recombination Noise in Double-Heterojunction Bipolar Transistors," IEEE Elec. Dev. Lett. EDL-5, 277 (1984).

1985

188. N. Chand, R. Fischer and H. Morkoc, "Collector-Emitter Offset Voltage in AlGaAs / GaAs Heterojunction Bipolar Transistors," Appl. Phys. Lett. 47, 313 (1985).

189. N. Chand, T. Henderson, R. Fischer, W. Kopp, H. Morkoc and L. J. Giacoletto, "A pnp AlGaAs / GaAs Heterojunction Bipolar Transistor," Appl. Phys. Lett. 46, 302 (1985).

190. N. Chand, P. A. Houston and P. N. Robson, "Gain of a Heterojunction Bipolar Phototransistor," IEEE Trans. - Elec. Dev. ED-32, 622 (1985).

191. N. Chand and H. Morkoc, "Doping Effects and Compositional Grading in $Al_xGa_{1-x}As$ / GaAs Heterojunction Bipolar Transistors," IEEE Trans. - Elec. Dev. ED-32, 1064 (1985).

192. R. Fischer, N. Chand, W. Kopp, H. Morkoc, L. P. Erickson and R. Youngman, "GaAs Bipolar Transistors Grown on (100) Si Substrates by Molecular Beam Epitaxy," Appl. Phys. Lett. 47, 397 (1985).

193. T. Ishibashi, H. Ito and T. Sugeta, "Luminescence of Hot Carriers in the Base of an ALGaAs / GaAs HBT," Inst. Phys. Conf. Ser. 74, 593 (1985).

194. H. Ito, T. Ishibashi and T. Sugeta, "Current Gain in Graded Base AlGaAs / GaAs HBTs Associated with Electron Drift Motion," Jap. J. Appl. Phys. 24, L241 (1985).

195. B. Kim, H. Q. Tserng, S. K. Tiku and H. D. Shih, "AlGaAs / GaAs Heterojunction Bipolar Power Transistors," Elect. Lett. 21, 258 (1985).

196. M. Kurata, R. Katoh and J. Yoshida, "Ring Oscillator Circuit Simulation with Physical Model for GaAs / GaAlAs Heterojunction Bipolar Transistors," IEEE Trans. - Elec. Dev. ED-32, 1086 (1985).

197. S-C. Lee, J-N. Kau and H-H. Lin, "Current Transport Across the Emitter-Base Potential Spike in AlGaAs / GaAs Heterojunction Bipolar Transistors," J. Appl. Phys. 58, 890 (1985).

198. H-H. Lin and S-C. Lee, "Direct Measurement of the Potential Spike Energy in AlGaAs / GaAs Single-Heterojunction Bipolar Transistors," IEEE Elec. Dev. Lett. EDL-6, 431 (1985).

199. R. J. Malik, F. Capasso, R. A. Stall, R. A. Kiehl, R. W. Ryan, R. Wunder and C. G. Bethea, "High-Gain, High-Frequency AlGaAs / GaAs Graded Band-Gap Base Bipolar Transistors with a Be Diffusion Setback Layer in the Base," Appl. Phys. Lett. 46, 600 (1985).

200. M. J. Mondry and H. Kroemer, "Heterojunction Bipolar Transistor Using a (Ga,In)P Emitter on a GaAs Base, Grown by Molecular Beam Epitaxy," IEEE Trans. - Elec. Dev. Ed-32, 175 (1985).

201. P. Narazny and H. Beneking, "Double Heterojunction GaAs / GaAlAs I^2L Inverter," Elect. Lett. 21, 328 (1985).

202. J. Shibata, Y. Mori, Y. Sasai, N. Hase, H. Serizawa and T. Kajiwara, "Fundamental Characteristics of an InGaAsP / InP Laser Transistor," Elect. Lett. 21, 98 (1985).

203. L. M. Su, N. Grote, R. Kaumanns, W. Katzschner and H. G. Bach, "An InGaAsP / InP Double-Heterojunction Bipolar Transistor for Monolithic Integration with a 1.5-μm Laser Diode," IEEE Elec. Dev. Lett. EDL-6, 14 (1985).

204. L. M. Su, N. Grote, R. Kaumanns and H. Schroeter, "NpnN Double-Heterojunction Bipolar Transistor on InGaAsP / InP," Appl. Phys. Lett. 47, 28 (1985).

205. E. J. Zhu, R. Fischer, T. Henderson and H. Morkoc, "An Emitter Guard-Ring Structure for GaAs High-Gain Heterojunction Bipolar Transistors," IEEE Elec. Dev. Lett. EDL-6, 91 (1985).

I.E. OTHER DEVICE (INCLUDING FETs) BIBLIOGRAPHY

1980

206. D. Boccon-Gibod, J-P. Andre, P. Baudet and J-P. Hallais, "The Use of GaAs-(Ga,Al)As Heterostructures for FET Devices," IEEE Trans. - Elec. Dev. ED-27, 1141 (1980).

207. M. Heiblum, "Tunneling Hot Electron Transfer Amplifiers (THETA): A Proposal for Novel Amplifiers Operating in the Subpicosecond Range," IEDM - 1980, p. 629.

208. R. F. Leheny, R. E. Nahory, M. A. Pollack, A. A. Ballman, E. D. Beebe, J. C. Dewinter and R. J. Martin, "An $In_{.53}Ga_{.47}As$ Junction Field-Effect Transistor," IEEE Elec. Dev. Lett. EDL-1, 110 (1980).

209. H. Ohno, J. Barnard, C. C. Wood and L. F. Eastman, "Double Heterostructure $Ga_{0.47}In_{0.53}As$ MESFETs by MBE," IEEE Elec. Dev. Lett. EDL-1, 154 (1980).

1981

210. H. Beneking, N. Grote, W. Roth, L. M. Su and M. N. Svilans, "Realization of a Bipolar GaAs / GaAlAs Schottky-Collector Transistor," Inst. Phys. Conf. Ser. 56, 385 (1981).

211. M. Heiblum, "Tunneling Hot Electron Transfer Amplifiers (THETA): Amplifiers Operating Up to the Infrared," Solid State Elect. 24, 343 (1981).

1982

212. R. C. Clarke, H. C. Nathanson, J. G. Oakes and G. T. Hardison, "GaAs High Power X-Band Vertical MESFET," IEEE Trans. - Elec. Dev. ED-29, 1709 (1982).

213. J. A. Cooper, F. Capasso and K. K. Thornber, "Semiconductor Structures for Repeated Velocity Overshoot," IEEE Elec. Dev. Lett. EDL-3, 407 (1982).

214. J. Y. Tang, K. Hess, G. J. Iafrate and R. Malik, "High Energy Injection and Transient Electron Transport in Gallium Arsenide," IEEE Trans. - Elec. Dev. ED-29, 1710 (1982).

1983

215. F. Capasso, "Band-Gap Engineering via Graded Gap, Superlattice, and Periodic Doping Structures: Applications to Novel Photodetectors and Other Devices," J. Vac. Sci. Tech. B 1, 457 (1983).

216. E. Kohn, U. Mishra and L. F. Eastman, "Short-Channel Effects in 0.5- μm Source-Drain Spaced Vertical GaAs FETs -- A First Experimental Investigation," IEEE Elec. Dev. Lett. EDL-4, 125 (1983).

217. H. Mader, R. Müller and W. Beinvogl, "Bulk-Barrier Transistor," IEEE Trans. - Elec. Dev. ED-30, 1380 (1983).

1984

218. P. M. Campbell, W. Garwacki, A. R. Sears, P. Menditto and B. J. Baliga, " Trapezoidal-Groove Schottky-Gate Vertical GaAs FET (GaAs Static Induction Transistor)," IEDM - 1984, p. 186.

219. Z. H. Chen, J. S. Smith, S. Margalit, A. Yariv and L. C. Chiu, "Proposed GaAs-Al-GaAs Metal Base Transistor," Jap. J. Appl. Phys. 23, L238 (1984).

220. L. F. Eastman, P. Maki and J. Wendt, "Structures for High Frequency Transistors. Part I: Vertical Schottky-Gated Transistors with Ballistic Electron Injection and Drift," Annual Report to DARPA, 1984.

221. C. Lyden and J. S. Campbell, "A Numerical Analysis of a Short Vertical n^+-n^--n^+ GaAs MESFET," IEEE Elec. Dev. Lett. EDL-5, 43 (1984).

222. U. Mishra, P. A. Maki, J. R. Wendt, W. Schaff, E. Kohn and L. F. Eastman, "Vertical Electron Transistor (VET) in GaAs with a Heterojunction (AlGaAs - GaAs) Cathode," Elect. Lett. 20, 145 (1984).

223. Z. Rav-Noy, L-T. Lu, E. Kapon, S. Mukai, S. Margalit and A. Yariv, "Vertical Field-Effect Transistors in III-V Semiconductors," Appl. Phys. Lett. 45, 258 (1984).

224. Z. Rav-Nay, U. Schreter, S. Mukai, E. Kapon, J. S. Smith, L. C. Chiu, S. Margalit and A. Yariv, "Vertical FETs in GaAs," IEEE Elec. Dev. Lett. EDL-5, 228 (1984).

225. N. Yokoyama, K. Imamura, T. Ohshima, H. Nishi, S. Muto, K. Kondo and S. Hiyamizu, "Tunneling Hot Electron Transistor Using GaAs / AlGaAs Heterojunctions," Jap. J. Appl. Phys. 23, L311 (1984).

1985

226. P. M. Campbell, W. Garwacki, A. R. Sears, P. Menditto and B. J. Baliga, "Trapezoidal-Groove Schottky-Gate Vertical Channel GaAs FET (GaAs Static Induction Transistor)," IEEE Elec. Dev. Lett. EDL-6, 304 (1985).

227. F. Capasso and R. A. Kiehl, "Resonant Tunneling Transistor with Quantum Well Base and High-Energy Injection: A New Negative Differential Resistance Device," J. Appl. Phys. 58, 1366 (1985).

228. C. Y. Chang, Y. H. Wang, W. C. Liu and S. A. Liao, "MBE Grown n^+ -i-$\delta(p^+)$-i-n^+ GaAs V-Groove Barrier Transistor," IEEE Elec. Dev. Lett. EDL-6, 123 (1985).

229. C. Y. Chang, Y. H. Wang, W. C. Liu, S. A. Liao and K. Y. Cheng, "Molecular Beam Epitaxially Grown Circular U-Groove Barrier Transistor," Appl. Phys. Lett. 46, 1084 (1985).

230. C. Y. Chen, A. Y. Cho and P. A. Garbinski, "A New $Ga_{.47}In_{.53}As$ Field-Effect Transistor with a Lattice-Mismatched GaAs Gate for High-Speed Circuits," IEEE Elec. Dev. Lett. EDL-6, 20 (1985).

231. N. Emeis and H. Beneking, "Fabrication of Widegap-Emitter Schottky-Collector Transistor Using GaInAs / InP," Elect. Lett. 21, 85 (1985).

232. W. R. Frensley, B. Bayraktaroglu, S. E. Campbell, H-D. Shih and R. E. Lehmann, "Design and Fabrication of a GaAs Vertical MESFET," IEEE Trans. - Elec. Dev. ED-32, 952 (1985).

This concluded the listing of the bibliographic library we have assembled, and completes Part I of this Technical Report. Items in this bibliography are referred to in Part II of this Report (which follows, starting on page 45) by a number in parentheses. Thus in the narrative that follows, a citation (136) would be to the paper by Hayes et al. listed on page 28.

Occasionally in Part II of this Report, and more frequently in Parts III and IV of the Report, it is necessary to refer to a published piece of work other than items in the high electron velocity bibliography just listed. Such a citation will be indicated in the text by a superscripted numeral, and the listing of those references is provided following Part IV, starting on page 102 of this Report.

II. Assessment of the literature to suggest guidelines for future DARPA-sponsored work.

This Part of the final technical report presents a broad overview of the literature listed in I. above. The goal of the research program has been to study the literature, examine carefully the assumptions made and experiments undertaken, and then to use this body of knowledge to suggest which directions of research might be most profitable. As discussed in the six-month report, our study of the literature has led us to believe that previously neglected scattering mechanisms limit the mean free path for electrons in GaAs to quite short distances - on the order of 400 angstroms. Since in a device such as an FET or MODFET, the electrons travel parallel to the surface (horizontally) the short distance between scattering collisions places extreme sub-micron demands on device lithography and processing.

Devices where the electrons travel perpendicular to the surface (vertically), such as bipolar transistors, do not suffer these same limitations. Even with current technology, it is quite routine to produce layer thicknesses on the order of a few hundred angstroms. Thus the short scattering length does not pose as serious a problem for the vertically oriented devices.

This Part is divided into three sections. In the first (Section II.A), we briefly recapitulate the arguments presented in the six month technical report that led us to believe that vertical devices offer greater promise. We then discuss the limitations to electronic velocity presented by various scatter-

ing mechanisms that may be present, as well as those presented by the material itself. The narrative continues by pointing out directions in which we feel that future research might be directed. Here we briefly discuss horizontal device structures, and deal extensively with three of the more promissing possibilities for vertical devices. Section II.C. discusses in some detail the permeable base transistor, the planar doped barrier transistor, and the heterojunction bipolar transistor. Several other device structures will also be mentioned.

II.A. Limitations due to scattering in GaAs.

There are several factors that limit the electron drift velocity in GaAs. Many of these factors are associated with scattering of the electrons. Several types of scattering are important and must be descussed. Traditionally, when velocity limitations due to scattering are discussed, three mechanisms are stressed: collisions with acoustic phonons through the deformation potential, collisions with polar optic phonons, and ionized impurity scattering. In addition to these well-known mechanisms, several other types of scattering are increasingly being recognized as playing an important role in determining the scattering length of electrons in GaAs, and thus the velocity.

Since we are concerned with the velocity of electrons in GaAs, it is necessary to be somewhat familiar with the structure of the conduction band in this material. As shown in Figure 1, this band is characterized by a direct minimum at the gamma point, with two higher valleys.[1] The L band, in the [111]

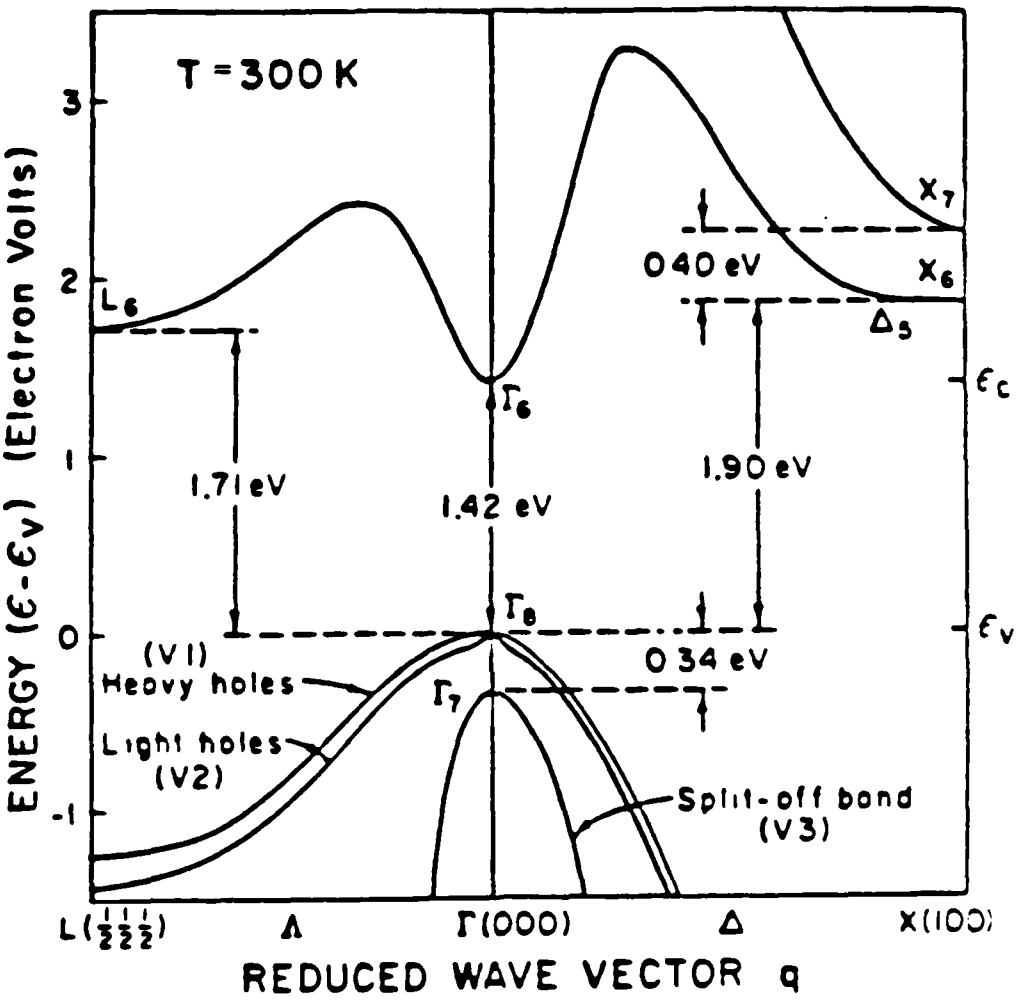


Figure 1. The uppermost valence bands and lower conduction bands of GaAs, from the 1982 review by Blakemore.[1] (Reference citations given as superscripts are described in the Reference list following Section IV of this Report.)

direction, has its minimum at about 0.36 eV above the gamma minimim, and the X band, in the [100] direction, is slightly higher than the L band. It is, of course, most favorable energetically for the electrons to be in the gamma band. However, scattering processes and the application of electric fields can cause appreciable fractions of the electronic population to reside in the L and X valleys. The sharply curved central minimum corresponds to an effective mass of only 0.063 m, where m is the free electron mass. The smaller curvature of the L and X valleys leads to effective masses of 0.22 m and 0.58 m respectively. Thus when electron are scattered from the gamma band to either of the two higher lying bands, the mobility suffers drastically. It becomes imperative, then, to keep as large a fraction of electrons as possible in the gamma band for as long as possible, if very high electronic velocities are to be realized.

Interband transfer of electrons is accomplished primarily by two mechanisms. In any type of device, the electrons will be under the influence of an electric field. The application of this field can give enough energy to electrons to boost significant numbers of them into the higher bands. The effect of the field on the upper valley populations in shown in Figure 2. Since the electronic states in these bands have lower mobilities, as greater numbers of electrons are raised to the higher valleys, the average electron velocity actually decreases. Thus the net effect is the well-known retrograde electron velocity-field

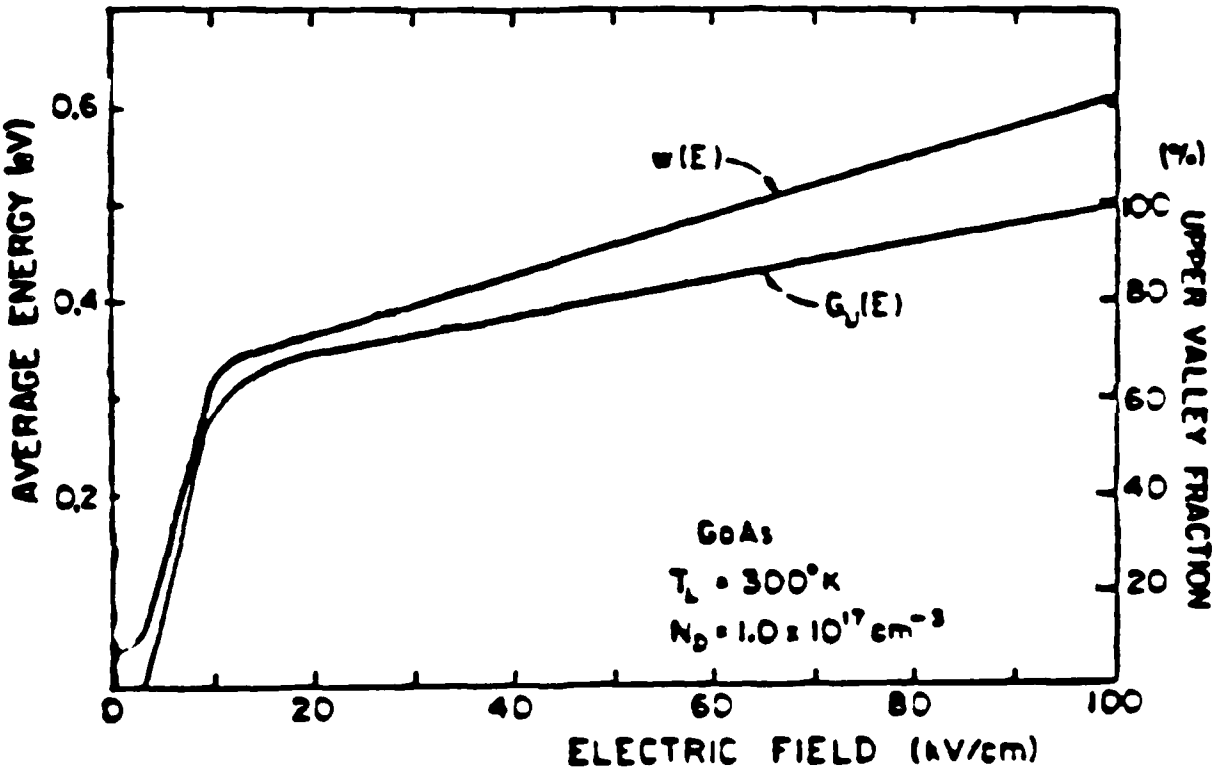


Figure 2. Fraction $G_u(E)$ of electrons in the upper valleys, and average electronic energy w(E), as functions of electric field. From Cook and Frey (57).

characteristic in GaAs. At low applied electric fields, the average velocity increases. Then, at higher fields, the velocity levels off, and the application of even higher fields causes a lowering of the average electronic velocity.

The second mechanism that often boosts electrons from the gamma valley to the upper ones is scattering. A large number of scattering mechanisms can be responsible. Among the most common are collisions with acoustic phonons through the deformation potential, collisions with polar optic phonons, and ionized impurity scattering (16). Recent experimental work has shown that several other mechanisms also play major roles in limiting the electronic velocity. These "new" scattering mechanisms primarily involve electron interactions with other electrons or plasmons, and will be discussed later.

One further restraint on the magnitude of the electronic velocity needs to be mentioned. By definition, the group velocity of electrons in a material is given by (dw/dk), where w is the angular frequency and k is the wave vector of the electrons. This can be written as $(1/\hbar)(dE/dk)$, which is just a constant times the slope of the E(k) relationship. Thus, the greater the slope (the first derivative), not the curvature (the second derivative), the higher will be the velocity of the electrons. For the conduction band of GaAs (shown in Figure 1), the maximum slope occurs at the gamma minimum in the [100] direction. This value of dE/dk corresponds to a maximum electronic velocity of 1×10^8 cm/s. This value presents the largest

velocity possible for electrons in GaAs. It places an upper limit on the claims of the theoretical calculations.

II.B. Theoretical and Experimental Reports on High Electronic Velocity in GaAs.

In this section, we will briefly mention some of the literature, both theoretical and experimental listed in the bibliography (Part I of this Report) concerning the possibilities for achieving very high electronic velocities. The theoretical work can be broken into two broad groups. The first involves primarily Monte Carlo types of calculation. The second group of models is based on a hydrodynamic interpretation of the Boltzmann Transport Equation. This first type of calculation is numerical. The second is analytical. In discussing the theoretical results, we will attempt to identify to which school the particular calculation belongs.

One of the earliest Monte Carlo predictions was made in 1972 by Ruch (5). His calculation, assuming that the dominant scattering mechanism was collisions with polar optic phonons, concluded that the electrons could reach a maximum speed of 4.7 x 10^7 cm/s. Carnez et al. claimed that by using pulsed fields and with gate lengths of only 0.2 micron, the electrons could reach a peak velocity of 8 x 10^7 cm/s (25). Shur and Eastman discussed the possibility of injecting electrons that already had a considerable amount of energy - some value less than the 0.36 eV difference between the gamma and L bands (21). Their calculation, an analytical one, predicted top speeds in the mid 107

range for devices at 77 K. From their model, they inferred that ballistic transport, i.e., transport without collision was feasible at low temperatures where there are few phonons.

The first experimental evidence to the contrary was also provided by Eastman's group (26). They found that the polar optical phonons limited the electronic mean free path to about 0.1 - 0.2 micron. Shank et al. measured a similar 0.2 micron path length for an AlGaAs - GaAs heterostructure (52). The measurement, which was done at 77 K, revealed a maximum electronic velocity of about 4×10^7 cm/s.

The relatively scarce experimental data has continued to reveal electronic velocities considerably lower than the early predictions. As a result, some of the more recent calculations have tended to be less optimistic. Littlejohn et al., in 1983, used a Monte Carlo calculation to find that even if electrons are injected with energies less than the intervalley energy of 0.36 eV, a significant proportion of the electrons will still scatter into the upper valleys (133). These ballistically launched electrons tend to lose their momentum very rapidly - on the order of a few hundred angstroms, not the few thousand angstroms previously assumed. One of the main reasons for the larger than expected number of electrons residing in the upper valleys is due to the pileup of charge that always seems to accumulate at the drain end of the channel. This phenomenom, pointed out by Awano (86) and shown in Figure 3, could lead to increased electron - electron interactions. Recent Monte Carlo studies by Lugli and

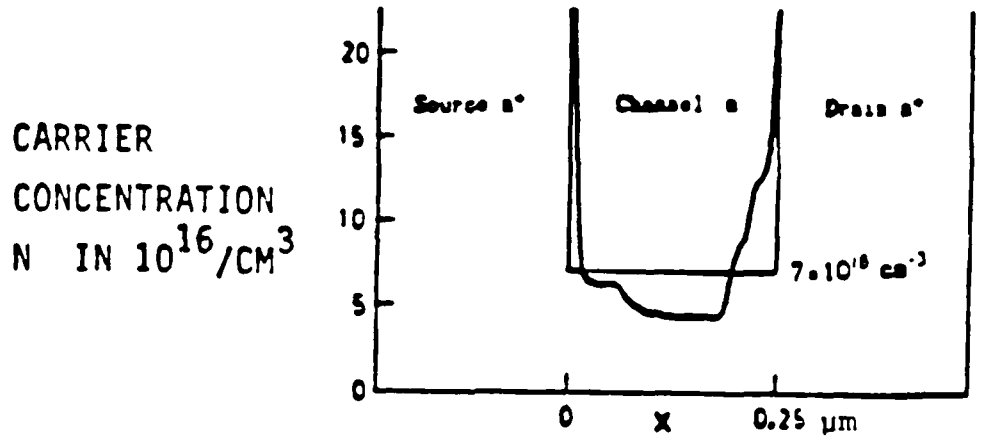


Figure 3. Results of Awano et al. (86) in Monte Carlo modeling of the variation of carrier density along the length of a short-channel (0.25 µm) FET. Note the carrier pile-up towards the drain end.

Ferry (137)have shown that if these interactions are taken into account, the possibility for ballistic transport is eliminated except for very short distances.

The most recent experimental work has confirmed this diagnosis. Using a vertically oriented device where the electrons flow perpendicular to the surface (we will report on this type of device in Section II.C. of this Report), Hollis et al. found that both electron - electron scattering and coupled plasmon - optical phonon scattering exhibited a greater influence on the electronic velocity than did the polar optical phonon scattering that had been previously thought to be the major culprit (131). Work by Hayes et al. has also shown that the electron - electron scattering is a major barrier to ballistic transport over long distances (136). They found considerable scattering in a vertical device with a base length of 1200 angstroms, and calculated that the mean free path between collisions was actually only about 400 angstroms.

It has become increasingly clear as the device fabrication technology has improved, that the results of the electronic velocity measurements cannot meet the early predictions. As device geometries shrink, the large number of electrons present in the active region tends to cause the transport to be space charge limited. Coulombic interactions between electrons and plasmons, and among electrons themselves tend to be the dominant scattering mechanisms and limit the range of very rapid electron transport to lengths of only a few hundred angstroms. Unless

fabrication technology increases dramatically, so that lithographic definition of lengths of this magnitude can be made, it appears that the horizontal MESFET/MODFET geometry cannot utilize the full potential of the higher electronic velocities possible in GaAs.

Since it is much easier (and indeed easily possible with technology currently available) to fabricate vertical layers several hundred angstroms thick, we feel that the fastest devices of the future will be vertically oriented - that is, with the electron flow perpendicular to the surface. While it is true that lithographic definition distances have improved significantly in recent years, it appears that it will always be possible to fabricate an active layer thinner than one definable horizontally by lithographic techniques. Since we see these vertical devices as being the most promising for the future, the second half of our study and the remainder of Part II of this Report deal with specific vertically oriented device structures, and their strengths and weaknesses.

II.C. Promising Device Structures for Future Work.

In the previous section of this Report, we detailed some of the evidence that has convinced us that the most promising device structures for future work are vertically oriented ones. In this section, we will describe three of these structures in some detail, stressing both the strengths and weaknesses of each approach. We will also briefly mention several of the less well known devices. Since we are limiting ourselves to vertical

devices, we will not report on the vast sea of information available concerning either GaAs MESFETs or the various HEMT or MODFET structures. Although much work is currently being carried out on both of these device types, we feel that that is primarily due to the fact that both utilize currently available technology. As these horizontal devices are fabricated and continue to be less than spectacular in their performance, we feel that workers in the field will begin to explore some of the vertical devices more seriously, even though new fabrication technology must be developed.

This section of Part II will be divided into four subsections, dealing with permeable base transistors, planar doped barrier transistors, heterojunction bipolar transistors, and other devices, respectively. In each subsection, some of the seminal work will be cited. Other references concerning the various structures can be found in the bibliography listed in Part I of this Report. We have concentrated on the three device structures mentioned above because the bulk of the work to date has dealt with them. Thus, they present the future possibilities that are closest to realization.

II.C.1. Permeable Base Transistor. The permeable base transistor is a device structure in which the "base" consists of a grid of tungsten fingers actually embedded directly in the GaAs material. These fingers act in a manner analagous to the grid of a vacuum tube triode. The relevant geometry is shown in Figure 4. First fabricated at Lincoln Laboratories in 1980 (107),

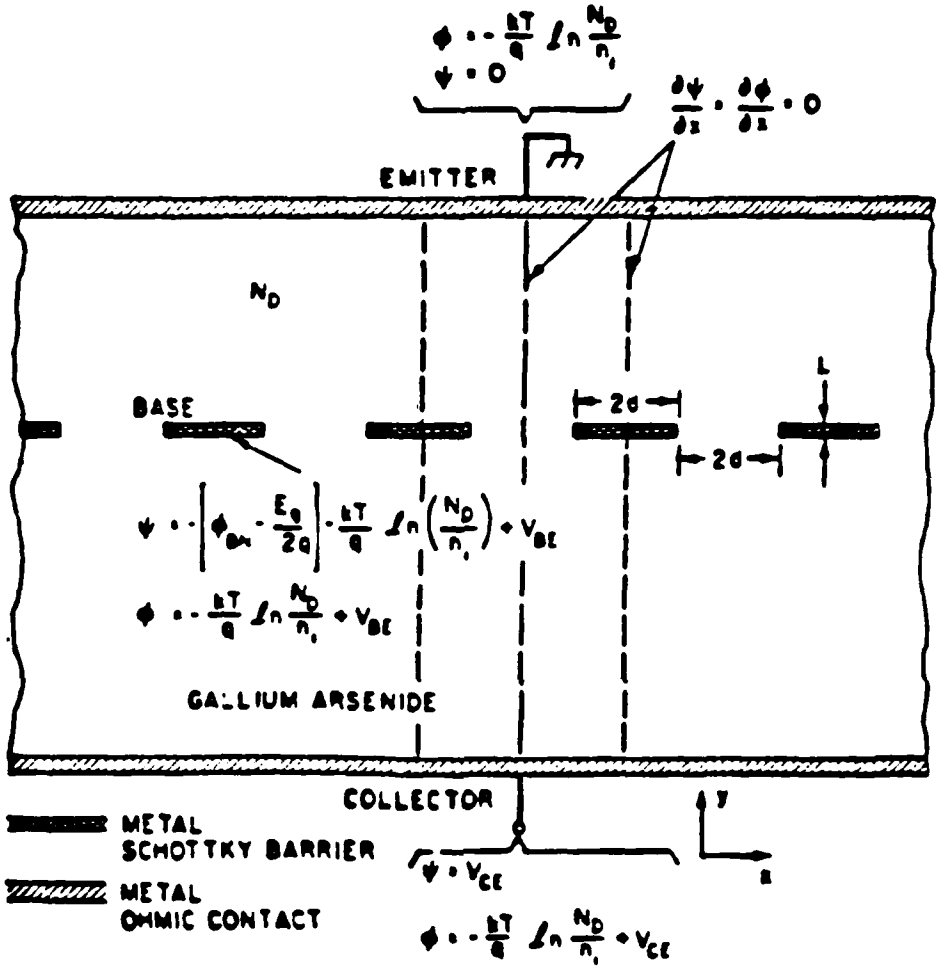


Figure 4. Device geometry of the permeable base transistor, from Bozler and Alley (108). A tungsten grating is embedded in the GaAs, and the electrons must pass through slits in this grating.

permeable base transistors have ben studied primarily there and at Nippon Telephone and Telegraph Laboratories in Japan (116).

The devices are fabricated by first growing an n-type layer on the n+ GaAs substrate. A series of tungsten lines 1600 angstroms wide and 300 angstroms thick is then deposited using electron beam evaporation. Since the lines are so narrow, x-ray lithography and liftoff techniques must be used. A second tungsten film is tnen deposited to form shorting bars between the tungsten fingers. This much larger deposition can be done with conventional lithographic techniques. Finally, a second n-type layer of GaAs is grown around and over the tungsten grating. Tungsten is sufficiently inert to GaAs that epitaxial growth can take place around the fingers without significantly affecting the electrical properties of either the GaAs or the tungsten.

The embedded grating forms a Schottky barrier with the the GaAs, which forms the base of the transistor. By applying a potential to the tungsten base, a potential barrier may be raised or lowered in the region af GaAs that is between the grating fingers. Thus the flow of electrons between the emitter and collector can be easily controlled. The permeable base transistor, then, acts like a vertical FET. With small enough tungsten fingers, this type of device should be capable of achieving very high speeds.

Although the permeable base transistor has the advantage of being conceptually very simple it suffers from several serious problems. The principal difficulty is connected with the

fabrication of the tungsten grating. Higher switching speeds can be achieved only by reducing the size of the fingers and the spacing between them. The devices which have been fabricated to date have generally had both the finger width and the spacing between adjacent fingers equal to about 1600 - 2000 angstroms. To achieve this type of accuracy has actually pushed the state of the art in lithography. X-ray techniques have been required, since the wavelengths used in conventional lithographic processes are considerably larger than the dimensions involved. In addition to the extremely small dimensions desired, the spacing between fingers must also be as uniform as possible. This spacing is primarily responsible for determining the threshold voltage of the device. Since for VLSI applications, it is necessary for the devices comprising a single chip to have as uniform as possible threshold voltage, this constraint is also crucial.

So while the permeable base transistor overcomes the electron scattering length problem by having the electrons travel vertically, the device properties are still governed by the constraints of horizontal lithography. Even by using state of the art x-ray optics, it may not be possible to push the dimensions much smaller than the 1600 angstroms presently available. Thus this particular device structure, while solving some of the problems, fails to overcome all of the barriers to achieving ultrahigh speed electron transport.

II.C.2. Planar Doped Barrier Transistor. The planar doped barrier transistor, shown in Figure 5, is a multi-layer device which utilizes two unipolar homojunctions. The first (the emitter) acts to inject electrons with a considerable amount of energy into a narrow base region, while the second functions as an energy analyzer (the collector), and transports only those electrons that have sufficient kinetic energy to surmount it. This device, essentially an n-i-p-i-n structure, was first grown by the Cornell group using molecular beam epitaxy, in 1980 (125). The p-type base will usually be fully depleted, and at zero bias, narrow space charge regions will be induced in the two n-type regions.

One key feature of the planar doped barrier transistor is that the emitter barrier height can be continuously varied from zero to approximately the band gap of the material. In practice, it is usually made to be about 0.35 eV high, so that electrons that are accelerated by it are not immediately scattered into the upper valleys in GaAs. The second barrier is biased so that only the "hot" electrons that have been injected by the emitter can surmount it. Low energy electrons that do not go over (or tunnel through) the collector barrier remain in the base region which is doped p-type, and quickly recombine. So current transport is achieved predominantly by well-behaved majority carrier thermionic emission over a barrier rather than the tunneling mechanism employed by Schottky barrier lowering. An additional attraction of this structure is that, unlike the heterojunction devices to

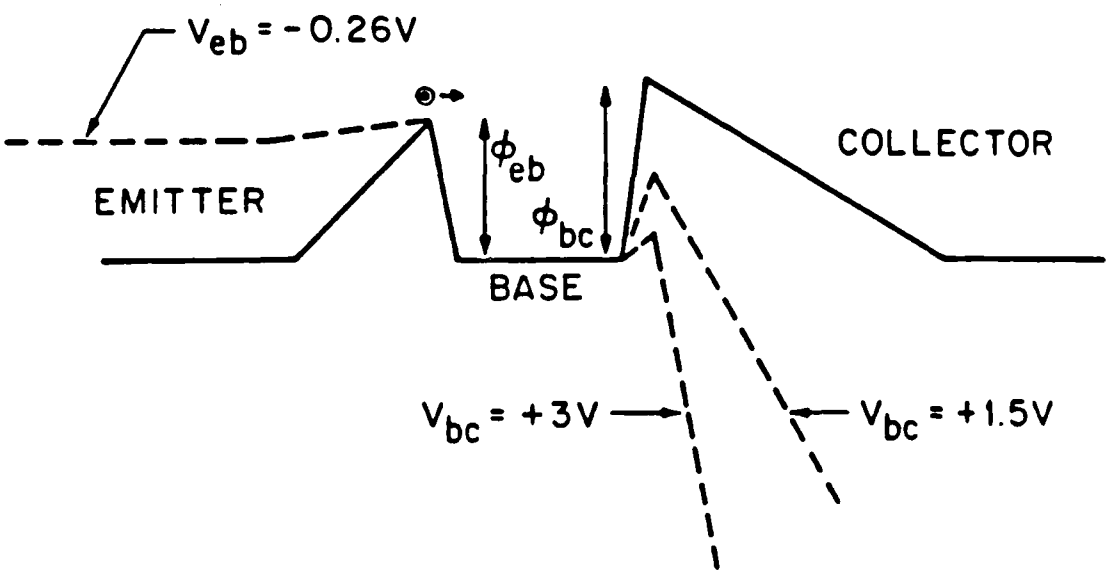


Figure 5. Energy diagram for a planar doped barrier transistor. The emitter-base junction is the hot electron injector, providing electrons of kinetic energy ϕ_{eb}. The base is the transit region, and the base-collector junction acts as a hot electron analyzer, rejecting electrons of K.E. < ϕ_{bc}. The dashed lines indicate the effect of V_{bc} on this barrier height and shape. From Hayes et al. (136).

be discussed in Section II.C.3., it is formed from a single semiconductor material, and thus avoids the problems of charge trapping, surface recombination, and thermal and lattice mismatch associated with interfaces between dissimilar materials.

Littlejohn et al. have made Monte Carlo calculations simulating the transport of electrons through planar doped barrier devices (133). They found that the average velocities possible in these devices should be substantially higher than the static drift velocity corresponding to the average value of the electric field in the device.

The behavior of the actual transistors, however, has been less impressive. The Cornell group attributes the poor common base current gain to the buildup of charge mentioned above. The large charge density leads to previously overlooked electron scattering with other electrons and with coupled plasmon-optical phonon modes. Even with base regions as short as 870 angstroms, noticeable scattering was present. Devices were also fabricated at Bell Laboratories by Hayes et al. (134,136). They used lower injection energies (emitter barrier of only 0.25 eV) and wider base regions - 1200 and 1700 angstroms. They also reported significant scattering, with, as to be expected, a greater amount of scattering in the longer-base device. From their measurements, Hayes et al. estimated that the electronic mean free path was only on the order of a few hundred angstroms.

The planar doped barrier transistor appears to offer a realistic approach to achieving a device with very high elec-

tronic transport velocities. It suffers from none of the technological problems encountered with the permeable base transistor. The major difficulty with this approach lies in the previously under-estimated electron scattering in the base region due to the increased charge density there. This scattering reduces the distance between collision to only a few hundred angstroms. While it would be possible to reduce the base length further, this would not entirely solve the problem. Even at 870 angstroms, the p-type base is fully depleted. If the base were made shorter, the space charge region would extend further into the n-type collector and emitter barriers, thus causing greater amounts of scattering in those regions. This would tend to reduce both the current gain of the device and its frequency response. So, while the planar doped barrier transistor appears to be promising, and is certainly worthy of further study, it may not be the final best solution.

II.C.3. Heterojunction Bipolar Transistor. It has long been suspected that a bipolar transistor with the emitter made from a material with a wider band gap than the material of the base and collector offers advantages in terms of speed and power consumption over transistorsmade entirely from a single material. Indeed Shockley applied for a patent for this idea in 1948! So although the idea was explored theoretically quite early, it wasn't until the early 1970s that the technology existed to attempt fabrication of heterojunction devices. First efforts, using LPE techniques, attempted to grow GaAs or ZnSe on

germanium. Due to numerous problems, such as lack of control over the doping profile in the junction caused by cross-doping, none of these early efforts proved particularly successful. In order to avoid these cross-doping problems, Dumke et al. first proposed working with the AlGaAs - GaAs system in 1972 (142). Other efforts, also using LPE growth techniques, soon followed (143). Since the mid 1970s, the advent of new epitaxial growth techniques such as MBE and MOCVD, has led to rapid improvement in III-V semiconductor epitaxial growth and thus increased interest in heterojunction transistors. For a review of the history of this type of device, see (155).

In a bipolar transistor, the flow of both the electrons and the holes must be controlled. In a uniform-gap semiconductor, the slopes of the two band edges are equal, so the forces on the two types of carrier are equal in magnitude and opposite in sign. In a heterostructure, the band gap may vary. Thus the two band edges and the forces on the carriers need not be the same. By using judicious combinations of energy gap variations and applied fields, it can become possible to control the forces acting on the electrons and holes independently of each other.

The theory behind the wide gap emitter is quite simple. Consider an n-p-n heterojunction transistor, the energy band diagram of which is shown in Figure 6. The large barrier in the valence band effectively prevents any holes from the p-type base from reaching the n-type AlGaAs emitter, regardless of how strongly the base is doped. The smaller band offset in the

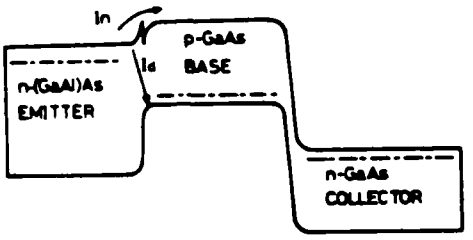


Figure 6. Energy band diagram for a $Al_xGa_{1-x}As/GaAs$ n-p-n heterojunction bipolar transistor (HBT), from Konagai and Takahashi (143). Note the spike in the conduction band energy at the AlGaAs-GaAs emitter-base heterojunction. As discussed in the text, one can also make the base-collector junction a heterojunction, and there is then also the possibility of a spike in energy at that location. Compositional and doping profiling methods are under investigation to minimize such spikes.

conduction band allows the electrons from the emitter to be injected with only a minor loss of efficiency. The carriers tend to be confined to the base region. Even if the doping levels in the base and emitter are high and low, respectively, and injection efficiency of nearly unity can still be maintained. These consequences yield a higher gain-bandwidth product due to the reduced base resistance.

While the use of a wide gap emitter has been expected to improve the performance of bipolar transistors for some time, the use of a wide gap collector also has recently been investigated. The advantages in this double heterojunction type of device are twofold. First, by using identical composition and doping in both the emitter and collector, these two components of the transistor can be effectively interchanged (174). This interchangeabliity can be important in IC design applications. in addition, a wide gap collector can minimize hole injection into the base, thus reducing the turn-on voltage, and consequently the power consumption (163).

There are, of course, problems associated with heterojunction bipolar transistors. As mentioned above, one of the early problems was cross-doping, where carriers from the heavily doped base diffused into the emitter. By using appropriate materials, and, more importantly, utilizing growth methods such as MBE and MOCVD where the temperature is kept fairly low, this problem has been largely solved.

A more serious problem lies in the fact that when the

heterojunctions are formed, a potential spike is formed in the conduction band at the emitter-base junction (181). This spike in the potential leads to a large collector offset voltage, which in turn, leads to a larger power consumption (197,198). The spike can be reduced to some extent by using either a graded gap base (159) or compositional grading near the heterojunction interface (155). When working with a double heterojunction device, a potential spike can also occur at the base - collector interface (204).

Currently several research groups are attempting to fabricate heterojunction bipolar transistors. The results have not been entirely successful. The primary problem appears to be related to the interface between the wide gap emitter and the narrower gap base. Due to structural problems on an atomic scale, such as thermal and lattice mismatch, flaw states are created. This leads to a large amount of electron trapping at the interface, with subsequent degradation of the transistor gain and frequency response. This problem, however, appears to be at least partially related to the growth of the structure. As noted above, techniques have been developed to reduce the potential spike that occurs at the interface. It is assumed that as the growth and fabrication processes improve, through improvements and better understanding of such techniques such as MOCVD and MBE, the interfacial trapping problem can also be reduced.

It should be pointed out that, while most of the experimental effort has been expended on the AlGaAs - GaAs system, other

III - V semiconductor alloys are also being currently studied. The InGaAsP - InP system has been used for not only for opto-electronics, but also for Heterojunction bipolar transistors (183,202-204), as has the InGaAs - InP system (172,178,182). Both GaInP (200) and AlInAs (161) have been used as the wide gap emitter in GaAs devices. The group at the University of Illinois has even worked with GaAs as an emitter on Si (192).

We feel, then, that the heterojunction bipolar transistor offers great promise for the future. As with the permeable base transistor, there are currently some technological problems in the fabrication of the devices, but unlike the case for that device, the problems associsted with the heterojunction bipolar transistor appear to be surmountable. We think that as growth techniques continue to improve, the interfacial trapping problem will be greatly minimized. However, much work still remains to be done before this type of structure can be routinely fabricated with uniform properties and high yields, for very high speed applications.

II.C.4. Other Possible Device Structures. Most of the work done on vertically oriented structures has been concerned with one of the three device types discussed above. There have also been numerous attempts to achieve high-speed devices using different vertical approaches. In this section we will very briefly describe some of these efforts, listing references where more detailed information can be obtained.

Tunneling hot electron transistors have been fabricated using epitaxial layers of GaAs and AlGaAs (225). Both the emitter and base layers are made of GaAs, but the electrons tunnel through a AlGaAs potential barrier between them. The electrons, then, are injected into the base with considerable energy. Scattering occurs in the base. A second potential barrier of AlGaAs is surmounted only by the unscattered "hot" electrons to reach the collector (207,211). So this device is similar to the planar doped barrier transistor, but here the barriers are due to layers of AlGaAs, and cannot be changed by biasing. The best devices fabricated so far have a transfer efficiency of only 0.28.

Schottky collector bipolar transistors have been made with wide gap emitters in both the AlGaAs - GaAs (210) system and the GaInP - InP system (231). One of the speed limitations to any bipolar transistor is the minority carrier storage time delay in the base. By using a metal-semiconductor, Schottky junction as the collector, fewer minority carriers are injected into the base and the problem is minimized. While the use of a wide gap emitter allows the base to be more heavily doped, thus reducing its resistance (see Section II.C.3. above), the base doping level determines the breakdown voltage of the Schottky collector junction as well.

An interesting class of device structures that utilize repeated velocity overshoot have been investigated recently by Bell Laboratories workers (213,215). These devices are layered

structures using a stairstep potential corresponding to a series of high-field regions separated by regions of lower field. The electrons will be accelerated in the high field regions which are short enough so that the transit time is less than the scattering time. Scattering, and its subsequent momentum loss, will take place in the low field region. So the average electron velocity will gradually become smaller there. However, a short while later, the electrons encounter another region of high field, and are accelerated once again. The spacing of the low field regions is determined by the scattering time also. The electrons must lose enough energy that the upper valleys do not become populated.

One of the difficulties of the permeable base transistor is the growth of GaAs over the tungsten fingers. In an effort to get around that problem, workers at General Electric have replaced the tungsten with fingers of p-type GaAs (218,226). The fingers in this trapezoidal groove, Schottky gate device are formed by ion implantation. As was the case with the permeable base transistor, however, the problem of horizontal lithography constraints remains to be solved.

The major attraction of the heterojunction bipolar transistor was that it allowed the use of a heavily-doped base, thus lowering the base resistance significantly. A (somewhat) logical extension of this line of thought is to replace the base with a layer of metal having an extremely low resistance. A GaAs - Al - GaAs, metal base transistor has recently been proposed (219).

With essentially no base resistance, these devices should operate at very high frequencies. Primarily due to the rather rough metal - semiconductor interfaces, early efforts to fabricate this type of structure have not been particularly encouraging.

The Cornell group has fabricated vertical unipolar transistors in GaAs using an AlGaAs cathode (220,222). The abrupt discontinuity in band gap between the two materials allows the electrons to be launched into the GaAs with considerable energy. Once in the GaAs, they are both accelerated by the field and slowed by collisions as in a horizontal FET. These first attempts have poorer results than expected, primarily because the scattering in the GaAs region was greater than predicted. By reducing the length of this region, improvement should be possible.

Several workers have proposed "vertical FETs" (212,216,221, 223,224,226,232) of various designs. The devices can be fabricated in a variety of ways, either using GaAs alone or AlGaAs - GaAs heterostructures. To eliminate the problem of source-drain punchthrough, the doping level in the p-type layer should be high. This can result in a highly compensated channel which leads to reduced mobility for the electrons. One way to overcome this problem is to grow a thin n-type layer instead of relying on silicon implantation. This completely removes the restrictions on the doping level in both the p- and n-type FET layers (223).

Other device structures have also been proposed or fabricated which take advantage of the higher electronic velocity

available in GaAs. Many of them are cited in Section I.E. of this Report. We do not claim that our list is complete. We do feel, however, that we have discussed the structures that offer the greatest possibility for ultrahigh speed. In order to exploit the high electronic velocity potential of GaAs and its related compounds, we feel that new fabrication technologies need to be derived. Current fabrication technology, while capable of producing FETs that are superior to silicon devices, is simply not able to fully utilize the benefits of GaAs. While still needing considerable work, the heterojunction bipolar transistor appears to offer the most promising behavior for the future.

III. Data Collection and Assessment Concerning EL2 and other Extrinsic Properties of GaAs

The midgap electron trap known as EL2 (formerly and erroneously known as "oxygen", and given the EL2 name as "electron trap #2" in a 1977 paper by Martin et al.[2]) has attracted a vast literature in recent years; probably with at least twice as many published papers as in our bibliographic listing in Part I for electron velocity phenomena. Despite these 450 or more papers in the last eight years, the true atomic nature of EL2 remains at this writing a matter for speculation, modeling attempts, controversy even over experimental results - let alone the implications of those results - and a continuing series of claims for "true success", followed by a watering-down or retraction. It is known that this midgap level is a donor,[3] and it seems almost certain that EL2 is a purely native defect or defect complex. Recent work by Baraff and Schlüter[4] in calculating the energies for various kinds of elementary defect in GaAs (the two types of antisite, two types of vacancy, four types of interstitial) should help avoidance in the future of attempts to construct models based on energetically-impossible situations. In any event, the need for a better understanding of the high temperature defect chemistry of GaAs which can allow centers such as EL2 to form at a concentration approaching 1 ppma is an urgent one.[5]

While EL2 plays a role even in N-type conducting GaAs, and more demonstrably at the interface between a MESFET's conducting

channel and a semi-insulating substrate,[6] it is par excellence in semi-insulating (SI) GaAs that effects related to EL2 and other deep-level traps are most prominent. This has received attention in various of the conference series on Gallium Arsenide and Related Compounds,[7] and closer attention still in proceedings of the three biennial conferences on Semi-Insulating III-V Materials.[8-10] Thus the most comprehensive single paper about the experimental status of EL2 as of 1984 (and with, moreover, a very balanced presentation) is the paper in Ref. 10 by Makram-Ebeid et al.[11] That paper outlines the striking experimental properties of this center/complex, including the metastable condition observable at low temperatures.

Since the work summarized in Ref. 11, there have been many more EL2 papers, of course, including several presented at international conferences claiming to "solve the EL2 problem". Alas, these have tended not to live up to expectations. It has been recognized for several years that EL2 occurs when GaAs has been provided with non-stoichiometric opportunities for the formation of As-rich defects such as V_{Ga} and As_{Ga}. The properties of As_{Ga} antisites show significant similarities with those of EL2 itself, as demonstrated for example by photo-ESR characteristics of antisites;[12] and this has led to a number of assertions that EL2 is the isolated antisite.[13,14] However, delicate ESR-tagged magnetic circular dichroism experiments[15] indicate that most As_{Ga} antisites in GaAs are apt to have a distorted environment indicating participation in a 2-site (or larger!) complex. One simple type of complex would be As_{Ga} with a vacancy nearby; not

apparently as a first-nearest-neighbor, but in the second through fourth shells of neighbor sites.

The question has, indeed, arisen as to whether or not EL2 is any specific type of defect/complex that can be fingerprinted. The experiments reported in papers by Ikoma and his University of Tokyo group[16] indicate a "family" of EL2 defects, with similar but not identical characteristics; and Martin[17] presented arguments at a 1985 conference as to why something with the properties of EL2 might be a complex with As_{Ga} as one component, and the second component (or other components) at distances of up to several nm. If EL2 is indeed such a nonunique collection of defect complexes, the sharp disagreemnts between various experimentalists as to what they think they have detected would be entirely predictable. The reader is reminded that many of the "F-center" types of defect in alkali halides never were adequately explained; people just eventually moved away to more tractable research problems.

One important difference between alkali halide research and the study of EL2 (and other extrinsic variables) in GaAs is that the latter material is of rapidly growing technological importance. If an aspect of GaAs's defect chemistry can not be completely understood, it is vital that it be amenable to complete control, since the existence of SI GaAs grown by the "undoped LEC" method in a boron nitride crucible is, currently, determined by presence of EL2 in numbers larger than those of (predominantly carbon) shallow acceptors. Whereas there are many other kinds

of electronic defect present in GaAs (as detectable by methods such as DLTS in conducting material,[18] or PITS conductance spectroscopy in SI material,[19] the concentration level of EL2 is usually so much larger (typically from 10^{15} to 3×10^{16} cm^{-3}, depending on growth method, post-growth anneal, etc.) that EL2 becomes the deciding issue as to whether the material is SI, and can remain so throughout device processing.

The question of the identity of EL2 is thus far from being one of only academic interest. Lack of this knowledge is a negative factor in evaluating the rate at which large-scale applications for GaAs ICs (and other devices requiring a SI substrate) should be encouraged for implementation in both defense and commercial markets.

In the lack of a universally agreed upon model for the nature of EL2, the next best thing is agreement on how this defect (an essential one for the way SI GaAs is presently grown) can be controlled to be present in a desirable amount and with excellent homogeneity throughout a grown boule - and of course from boule to boule as well. Any commercial manufacturer wants the maximum possible portion of his product to be saleable, and any customer would like GaAs wafers he procures to be as uniform as possible in all significant extrinsic properties; over the area of a wafer, from wafer to wafer within a lot, and from lot to lot. One here enters a world of partial information and witheld information, since GaAs crystal growth managers (whether in captive organizations or commercial vendors) tend to release

no more information than is necessary to satisfy most customers. This means that information about growth rate, post-growth cooling regimen, subsequent post-growth anneals (either as full ingots, part-ingots, or wafers; and in vacuum, As vapor, AsH_3, etc.) is released to a very limited extent. That understandable but frustrating secrecy on the part of the GaAs crystal growth industry makes it difficult for the various parties involved to work synergistically towards a more complete understanding of what the thermal/mechanical history of GaAs causes, and what are the consequences.

The extrinsic properties of concern here for GaAs as a device medium are by no means restricted to EL2 itself, though that is one major variable for SI GaAs. Other considerations for SI GaAs include the concentration and spatial distribution of dislocations, the number and mobility of carriers, the contribution towards compensation and midgap Fermi energy pinning of shallow impurities such as carbon acceptors, any effects of growth-rate striations, etc., etc. Concern over the role dislocations may play for device properties (a subject strongly emphasized in some recent Japanese work,[20-23] but appearing less significant according to some US work,[24,25]) has led to considerable effort towards growth of SI with zero or far fewer dislocations; through indium doping,[26,27] or by growth in a magnetic field.[28]

It would be nice if GaAs was intrinsically strong enough to be grown in large monocrystal form dislocation-free - as has

been taken for granted in the silicon industry for years. Since GaAs is twice as heavy as Si, and has a high-temperature critical shear stress much smaller than Si, the introduction of dislocation slip while a crystal is growing is all too natural a state of affairs, as modeled for example by Jordan et al.[29] It does appear likely that inhibition of melt convection by application of a magnetic field during growth[28] can make the resulting GaAs crystal more homogeneous in terms of reducing growth striations, but this alone does not render GaAs proof against dislocation formation and climb in the as-grown but still hot condition. Hence considerable recent and present interest in isovalent element doping for "lattice hardening", with In_{Ga} incorporation reported[26,27] as one of the most effective when present in a concentration of $\sim 10^{20}$ cm^{-3} (i.e., $\sim$0.5% of the Ga atoms replaced by indium). Ehrenreich and Hirth[30] have pointed out that a 5-atom $InAs_4$ unit in a GaAs solvent results in a 7% bond length increase compared with $GaAs_4$, and find the lattice "hardening" to be a natural consequence of the strain fields emanating from these $InAs_4$ inclusions.

Incorporation of as much as 0.5% atomic of indium in GaAs is by no means a trivial technological task. Since In has a low segregation coefficient (Hobgood et al.[27] estimate $k \approx 0.1$, but other numbers have been quoted elsewhere), doping the melt with enough indium to provide adequate lattice hardening for the first part of a grown ingot will tend to result in excessive indium in the melt for the latter stages of growth. That can and often does result in polycrystal growth towards the tail end of the

ingot grown from a In-doped melt. If this be postponed by starting with less In in the melt, then the upper part of the ingot contains too little indium to "harden" against dislocation formation - and we have seen a number of examples of "In-doped" SI GaAs crystals with inadequate indium content in our own examination of GaAs wafers from various commercial and non-commercial suppliers.

A very important question related to the above discussion is: what does a dislocation do to a GaAs device? We have noted above the deduction made in a series of papers from Japanese laboratories[20-23] that a strong correlation exists between the threshold voltage V_{th} of a MESFET, and the proximity of a dislocation. The trend of V_{th} with distance to the closest dislocation was, however, found to be considerably less steep when the GaAs had received a long-period anneal. A legitimate question is thus: does the dislocation affect a MESFET directly, or is something else the actual cause? Note in this regard that Winston et al.[24] did not find a correlation of V_{th} with dislocation proximity in their work; while work in which we have participated[25] (and which is further reported in Part IV of this Report) found some wafers in which V_{th} and dislocation density N_D had similar spatial patterns, yet other wafers for which V_{th} and N_D were quite differently distributed across the wafer's area. In that work in which we participated,[25] V_{th} was in all cases spatially correlated with the concentration N° of neutral EL2, as measured by near-IR transmittance, using the calibration of

Martin[31] for the neutral EL2 optical cross-section $\sigma_o(h\nu)$. The point-by-point measurement procedure developed at the Oregon Graduate Center for optical transmittance determination of N° in polished wafers of normal IC thickness (0.5 mm) is described elsewhere[32] and in Part IV of this Report. Part IV also includes some representative wafer maps of N° and of device properties.

A tentative conclusion from wafer mapping studies at OGC (correlated with device work at Triquint Semiconductor) is that GaAs MESFET V_{th} is <u>directly</u> affected by the local N° value.[25] A device may well be sensitive to the <u>total</u> EL2 concentration (those compensated by carbon as well as those still holding an electron at midgap energy), but the near-IR absorption method measures predominantly the neutral species.[32] [Note that Chen <u>et al</u>.[33] find a linear trend of V_{th} with carbon concentration, when the latter is measured using the local vibrational mode (LVM) absorption band at 17 μm.] If a GaAs wafer is carefully mapped for dislocations, but not for EL2 (as was the case with the Japanese work[20-23] noted above) then only part of the essential evidence has been scrutinized - and the opportunity to confuse cause and effect exists.

Our tentative conclusion at this juncture is thus that a dislocation <u>may</u> play a role in affecting V_{th} only through its ability to serve as a source/sink for the point defects from which EL2 and other midgap electronic states arise. Dislocation climb in recently-solidified and still very hot GaAs leaves in its wake a debris of point defects: vacancies, interstitials, and antisites. These will then undergo further transformations

to an extent that depends strongly on the subsequent thermal history of the ingot. The calculations of Baraff and Schlüter[4] suggest that interstitials are too costly in energy to remain in existence unless the GaAs is rapidly quenched to a low temperature - a procedure never carried out in practice since that would result in an ingot so affected by strain that it would be apt to fly into fragments when one attempted to shape it and wafer it. A completed GaAs ingot is accordingly usually cooled slowly, and may be retained in the growth chamber at a high temperature for several hours after the completion of solidification - this often intended primarily as a strain-relief precaution rather than for defect-chemistry adjustment. Nevertheless, the latter also happens! It happens even more so if the crystal is subsequently ramped up to a high temperature for a long period anneal.[34-36] For then ample opportunity is provided for point defects to achieve thermodynamic equilibrium appropriate for the anneal temperature. If the anneal is too brief to allow such equilibrium to be achieved (and the rate for a crystal to undergo such change depends among other things on the availability of local dislocations), then N° depends on both N_D and the time-temperature cycle. However, if the anneal is lengthy enough, the final result should become independent of N_D; with a value for N° determined by the As:Ga ratio and the anneal temperature itself.

This should be true whether EL2 is (as some have asserted) an isolated As_{Ga} antisite, or whether it is a complex such as $As_{Ga} - V_{As}$, $As_{Ga} - V_{Ga}$, $V_{As} - As_{Ga} - V_{Ga}$, etc., etc. Indeed,

perhaps all of those strange entities just mentioned exist in finite concentrations, with the relative strengths determined by the As:Ga ratio. We thus consider that further basic studies of GaAs high temperature defect chemistry ought to be very valuable in illuminating methods by which the production of highly uniform high quality SI GaAs may be assured. The availability of dislocation-free GaAs (by indium doping, or any other methods) may sound attractive, but might in fact not be necessary for MESFET IC applications. (We know that any dislocation is bad news indeed for optoelectronic applications, but that lies outside our present terms of reference.)

One problem in trying to determine just which are the vital extrinsic variables for SI GaAs, and to what extent can defects and dislocated be tolerated for IC applications, is that evidence is gathered statistically rather than causally. One is not, for example, able to observe a shift of V_{th} as a specific dislocation is moved nearer or further. Instead, one assembles information about V_{th} for many devices, and compares this with mapping information about dislocation density N_D, neutral EL2 concentration N°, resistivity, carrier mobility, luminescence, etc., as measured over the area of the device wafer or a slab cut adjacent to that wafer. Separation of the true kernel of the truth from much chaff is, accordingly, a slow business, with many conflicting claims and counter-claims. Yet continuation of attempts to map hopefully important properties is necessary since more direct causal approaches exist only as "thought experiments".

With the encouragement of Dr. Richard Reynolds of DARPA, we have become involved in such mapping of properties, the experimental work itself being largely under the aegis of another program funded by NSF. Part IV of this Report gives some idea of the amount of GaAs wafer mapping work that has been reported in the recent published/conference literature, and reports also on mapping measurements made by us specifically to assist in the DARPA-funded effort.

IV. Mapping of EL2 and Other Extrinsic and Device Properties of Gallium Arsenide Wafers

As noted in Part III (on page 82), evidence concerning how a GaAs device may or may not be affected by various aspects of the material's extrinsic properties has to be gathered principally by statistical rather than direct causal study. One can determine causally how the operation of a FET is affected by the strength of implant dose coupled with the energy distribution of implanted ions, since these variables determine the depth and condutance of the channel. However, the influences of substrate properties such as EL2 concentration, carbon concentration, dislocations, etc., must be inferred from statistical analysis of many devices and much material.

Since one would like devices to be of high performance and of high uniformity over a wafer, from wafer to wafer, and from batch to batch, the mapping of a wafer's properties becomes a useful tool in that quest for information. Such mapping is especially useful from the device aspects if one can then fabricate devices in the wafer that has been mapped, and proceeds to map the properties of a device array extending over the wafer's area. As noted below, there have been a number of recent studies with that objective.

The question of devices laid aside for a moment, the mapping of extrinsic semiconductor variables throughout a wafer - or, better still, throughout an entire melt-grown ingot - can provide valuable information to the crystal grower as to how well his/her

growth technique is adapted to the production of uniformly high quality material. Thus comparison of maps for one extrinsic material property with another can be helpful towards the goal of making GaAs crystal growth an optimized near-science. Those who grow crystals may be offended by our choice of the term "near-science", but we hope they can take our view constructively that a full understanding of the high temperature defect chemistry of GaAs is a prerequisite to making this an exact science.

Section IV.A. is used to give an abbreviated listing of some recent published papers/conference presentations dealing with various aspects of GaAs wafer/slab extrinsic mapping. To keep this summary brief, complete citations are not given, but the indication of first author, year, and journal (or conference) will be enough to allow those who wish to locate any of these items.

The paragraph above refers to mapping of GaAs wafer/slabs, since in some instances the sample needed to be several millimeters thick, rather than the normal 0.4 to 0.6 mm thickness of a wafer intended for device fabrication. This has been true for studies of carbon concentration through the 17 μm absorption of C_{As} sites; and for the vast majority of measurements and qualitative observations of neutral EL2 through its near-IR absorption. Only the work carried out here,[5,25,32] and recent work by the Freiburg group,[37] has been able to measure EL2 absorption with wafers of "normal" thickness.

IV.A. Tables Summarizing Recent Literature on Mapping Various GaAs Extrinsic Variables throughout Wafer/Slab-like Samples; and of Related Wafer Mapping of Devices

The tables presented in this section reproduce and update the information provided as an appendix to the Interim (6-month) report for this project.

In order to fit the lines of print of the various tables into standard page width, the typed text has been reduced to 77% of its original size. It is believed that the resulting tables are still legible.

See Section IV.B, starting on page 91, for comments on the material in these Tables, and for examples of mapping work carried out in, or in collaboration with, our OGC program.

IV.A.1. Papers Reporting Spatial Variation Across a SI GaAs Wafer of Resistivity (or of "Leakage Current" Test for Intrinsic Photosensitivity

Authors	Published Conference or Journal	Publi-cation Date	Type and size of Crystals used	Results reported
Blunt	Evian Conf.	1982	50 mm LEC and HB wafers	Contour map from "dark spot" response
Grant et al.	" "	1982	50 mm LEC (HP)	Contour map
Matsumura et al.	J.J.A.P.	1983	50 mm LEC (HP)	Line scan (M-shape for ρ and photo-leakage)
Holmes et al.	A.P.L.	1983	75 mm LEC (HP)	Line scans
Mita et al.	A.P.L.	1983	50 mm LEC, & HB	Pseudo-3D plots, for photoresponse & leakage
Duseaux & Martin	Kah-nee-ta	1984	50 mm LEC, In-doped	Radial variation shown only
Rumsby et al.	" " "	1984	50 mm LEC, annealed	Line trace
Goutereaux et al.	Biarritz	1985	50 mm LEC (HP)	Mosaic plot of R_H (1.5 mm res.) compared with EL2
Hyuga	J.J.A.P.	1985	50 mm LEC (HP)	Plots of Hall coefficient as correlated with local dislocation density.
Tamura and Onuma	J.J.A.P.	1985	50 mm LEC (HP)	Radial plots of carrier mobility and resistivity compared with dislocation etch pit density.
Hyuga et al.	A.P.L.	1985	50 mm LEC (HP) (Incl. In-doped)	Diameter plots for carrier concentration, as correlated with dislocation density.

IV.A.2. Papers Describing Mapping of Dislocation Density* Throughout GaAs Wafers (usually SI LEC Wafers)

Authors	Published Conference or Journal	Publication Date	Type and size of Crystals used	Results Reported
(a) Based on Etch Pit Counting				
Grant et al.	Evian Conf.	1982	50 mm LEC (HP)	Mosaic map display of EPD
Bonnet et al.	" "	1982	50 mm LEC (HP)	Mosaic map of EPD
Holmes et al.	A.P.L.	1983	75 mm LEC (HP)	Radial line trace of EPD
Matsumura et al.	J.J.A.P.	1983	50 mm LEC (HP)	Line scan of EPD
Mita et al.	A.P.L.	1983	50 mm LEC & HB	Pseudo-3D plot of EPD
Holmes and Chen	J.A.P.	1984	75 mm LEC (HP)	Contour maps of EPD
Ponce et al.	Kah-nee-ta	1984	LEC (prob. LP)	Line scan
Peigen et al.	" " "	1984	60 mm LEF (LP)	Line scan
DiLorenzo et al.	" " "	1984	LEC, incl. In-doped	Contour plot, and full-wafer photos
Stirland et al.	" " "	1984	LEC	High-magnification TEM compared with EPD.
Makanishi et al.	ICSSDM, Kobe	1984	FEC, In-doped	Line scan
Hyuga	J.J.A.P.	1985	50 mm LEC	Local dislocation density correlated with carrier density, as from Hall coefficient.
Tamura and Onuma	J.J.A.P.	1985	50 mm LEC	Radial plots of resistivity and Hall mobility compared with local dislocation density.
Yamada	A.P.L.	1985	50 mm LEC	Photoelastic measurements of strain distribution (arising from dislocations) shown as matrix plots.
(b) Pictures and/or Traces from X-ray Topographs				
Brown et al.	Kah-nee-ta	1984	50 mm LEC (HP)	3 mm wafers used, slip bands shown
Ponce et al.	" " "	1984	LEC (prob. LP)	Transmission picture of full half-wafer
Leigh et al.	" " "	1984	50 mm LEC (HP)	0.3 mm wafers used for XRT, etc.
Strausser & Rosencwaig	" " "	1984	LEC	Thermal-wave image comp. with XRT for high-magn.

*Note that many of these investigations have used chemical etching of the GaAs surface to create and observe dislocation etch pits. The X-ray topographic method, for which the Table above shows just a handful of 1984 examples, is in fact now being vigorously studied in numerous laboratories. Much more literature is currently in press.

IV.A.3. Work Describing Variation of (Neutral) EL2 Concentration (N°) in SI GaAs Slabs or Wafers, from Near-IR Transmittance

Authors	Published Conference or Journal	Publication Date	Type of Crystal	Diameter (mm)	Thickness (mm)	Other Material Features	Form of Data Presentation
Holmes et al	Evian Conf.	1982	LEC (HP)	75	4		Radial line plot
Holmes et al.	A.P.L.,	1983	LEC (HP)	75	4		Radial line plot
Brozel et al.	A.P.L.	1983	LEC (HP)	50	5		Radial line plot; also vidicon micrograph
Holmes et al.	A.P.L.	1983	LEC (HP)	75	4		Contour plot (measurement sites on grid of 3 mm x 6 mm).
Skolnick et al.	J.Elect.Mat.	1984	LEC (HP)	50	5		High resolution vidicon pictures
Skolnick et al.	A.P.L.	1984	LEC (HP)	to 75	3		High resolution vidicon pictures
Holmes & Chen	J.A.P.	1984	LEC (HP)	75	4		Contour plots based on measured 3 mm x 3 mm grid of locations
Duseaux & Martin	Kah-nee-ta,	1984	LEC (HP)	50	4	In-doped	Mosaic plot (1.5 mm resolution)
Osaka & Hoshikawa	" " "	1984	VMLEC (HP)	75	?	Magn. field	Radial line plot only
Foulkes et al.	" " "	1984	LEC (HP)	50	5	In-doped	Vidicon pictures, med-high res.
Rumsby et al.	" " "	1984	LEC (HP)	50	5	Annealed	Radial line trace only
Holmes et al.	" " "	1984	LEC (HP)	75	4	Incl.Anneal	Contour plots; 3 x 6 mm resolution
Leigh et al.	" " "	1984	LEC (HP & LP)	50	5	Incl.Anneal	High resolution vidicon pictures
Dobrilla et al.	" " "	1984	LEC (HP)	50	0.5 & 5		Mosaic plots (1 mm resolution)
Kaufmann et al.	" " "	1984	LEC	50	4		Vidicon images, medium resolution
Brozel et al.	" " "	1984	LEC	50	5		Line scan only
Skolnick et al.	" " "	1984	LEC	56	3		High-resolution vidicon pictures
Wang	" " "	1984	LEC (LP)	60	4		Line scan only, 4 mm resolution
Brown et al.	" " "	1984	LEC (HP)	50	3		Vidicon micrograph
Brozel et al.	J.A.P.	1984	LEC (HP)	50	3 & 5		Line scans & vidicon pictures
Martin et al.	Biarritz	1985	LEC (HP)	50	4	In-doped	Mosaic plots before and after ingot anneal
Brozel et al.	Biarritz	1985	LEC (HP)	50	5		High-resolution vidicon micro-photos, attempt at stereo view.
Goutereaux et al.	Biarritz	1985	LEC (HP)	50	5		Mosaic plot, 1.5 mm resolution
Blakemore et al.	WOCSEMMAD (not Publ.)		LEC (HP)	50	0.5		Mosaic plot, 1 mm resolution, compared with device parameters
Dobrilla et al.	MRS/SFO	1985	LEC (HP)	50	0.5		Mosaic, 1 mm res., device comp.
Windschief et al.	A.P.L.	1985	LEC (HP)	50	0.5 - 4.0		Line scans repeated to build up 2-D picture of transmission.
Dobrilla & Blakemore	J.A.P.	1985	LEC(HP/LP)	50/75	0.5		Mosaic plot, 0.5 mm resolution.
Dobrilla et al.	MRS Mtg.	1985	LEC (HP)	50	0.5		Comparison of mosaic plots for EL2 with device properties.
Dobrilla & Blakemore	DRIP Symp.	1985	LEC(HP/LP)	50/75	0.5		Comparison of EL2 matrix plots with device properties.
Windschief et al.	DRIP Symp.	1985	LEC (HP)	50	0.5		Line scans repeated for 2-D plot.
Martin & Duseaux	DRIP Symp.	1985	LEC (HP)	50	5		Mosaic plots; anneal effects.

IV.A.4. Papers Reporting on the Spatial Dependence Across a GaAs Slab or Wafer (usually SI, and usually LEC=grown) of the Concentration of Carbon (and other shallow acceptors).*

Authors	Published Conference or Journal	Publication Date	Type and size of Crystals Used	Results Reported
Holmes et al.	Evian	1982	75 mm LEC (HP)	Radial line plot, from LVM absorption at 17 μm
Miyazawa et al.	A.P.L.	1984	50 mm LEC	Room temp. cathodoluminescence, line scans with high resolution (∿2 μm).
Yokogawa et al.	J.J.A.P.	1984	50 & 75 mm LEC	Mosaic plots of 4.2 K, 1.49 eV PL, 2 mm resolution
Duseaux and Martin	Kah-nee-ta	1984	50 mm LEC, In-doped	Reports uniform low carbon from LVM absorption
Kitihara et al.	" " "	1984	LEC and VPE layers	Line scans of PL at 1.494 eV (carbon) and at 1.490 eV (zinc) along (010) and (011) diameters
Leigh et al.	" " "	1984	50 mm LEC (HP)	4.2 K cathodoluminescence in SEM, with photos of 5 x 5 mm^2 samples, and detailed line scans at 1.514 eV (e-h, flat) and 1.494 eV (rugged)
Chin et al.	A.P.L.	1984	LEC and HGF	300 K cathodoluminescence micrographs
Yokogawa et al.	Biarritz	1985	50 & 75 mm LEC	Mosaic plots of 1.49 eV PL showing anneal effects
Kikuta et al.	Biarritz	1985	Undoped S.I.(LEC?)	Microfocussed laser spot used to generate high resolution PL image at 1.49 eV, compare with the PL images for 0.65 eV and 0.8 eV.
Warwick and Brown	A.P.L.	1985	LEC	High spatial resolution near bandgap PL images.
Homma et al.	J.A.P.	1985	Small crystals by in-situ synthesis	Radial plot of C_{As} by LVM absorption.
Chen et al.	A.P.L.	1985	75 mm LEC	Radial plots of C_{As} by LVM absorption, compared with V_{th} for FETs made in similar material.

*Some entries in the Table above concern detection of carbon from the C.B - acceptor luminescence associated with the C_{As} shallow acceptor. This inevitably samples carbon close to the surface, and sample thickness is irrelevant. Other entries are for work using the 17 μm LVM absorption of C_{As}, a nonelectronic phenomenon. Since that absorption is not strong, and for other reasons, such work to the present time has always used a GaAs slab several mm thick.

IV.A.5. Papers Reporting Variation Over a GaAs Wafer's Area of Device Parameters Such as V_{th} and I_{dss}*

Authors	Published Conference or Journal	Publication Date	Type and size of Crystals used	Results Reported
DiLorenzo et al.	Kah-nee-ta	1984	LEC, inc. In-doped	Mosaic plot of FET V_{th}
Takebe et al.	" " "	1984	75 mm LEC (Mod.P)	Mosaic plots for V_{th} and K
Lee et al.	" " "	1984	75 mm LEC (HP)	Pseudo-3D plots of V_{th} for FETs aligned along [010], [011], and [01$\bar{1}$] directions.
Winston et al.	" " "	1984	50 mm LEC, In-doped	Line plots of V_{th} for low-disloc. material
Yamazaki et al.	A.P.L.	1984	50 mm LEC, In-doped	Mosaic plots of V_{th} for low disloc. mtl.
Winston et al.	Biarritz	1985	75 mm LEC, In-doped	Concerned with dislocation proximity in low-disloc. material as affecting V_{th} and CL.
Takano et al.	J.J.A.P.	1985	50 mm LEC/HB	Radial plot for V_{th} compared with lattice strain resulting from stoichiometry variation.
Dobrilla et al.	A.P.L.	1985	50 mm LEC	Matrix plots of V_{th} and I_{dss}, for wafers that had previously been mapped for EL2, showing substantial correlation.
Dobrilla & Blakemore	DRIP Symp.	1985	50 mm LEC (HP/LP)	Correlation shown between device parameters and local EL2 concentration, by matrix plots.
Manishi et al.	DRIP Symp.	1985	HB & LEC	Device parameters correlated with proximity of dislocation, and effect of crystal anneal.
Chen et al.	A.P.L.	1985	75 mm LEC (HP)	Comparison of V_{th} for FETs with carbon conc. as measured by ^{12}CLVM IR absorption.

*Most of the studies noted in the Table above relate to parameters of MESFET devices fabricated by direct ion implantation into SI wafers. As can be seen from the entries above, most of the wafers so processed and subjected to device mapping were of LEC GaAs, usually of the undoped (no chromium) variety, and with several studies examining material that had been isovalently alloyed with indium to drastically lower the dislocation density.

IV.B. Experimental Wafer Mapping Studies at OGC

In late 1983, an experimental system was built at the Oregon Graduate Center for near-IR transmittance mapping of SI GaAs wafers, and several of the fruits of having that capability are noted in the Table on page 88. Our work was not under DARPA sponsorship at that time, though our efforts were (as noted on page 83) encouraged by Dr. Richard Reynolds of DARPA.

From the first, we placed a high priority on achieving enough precision in transmittance measurement to be able to detect the EL2-related absorption coefficient for a wafer of normal IC thickness. Our first results using this system were described at the 1984 Semi-Insulating III-V Materials conference,[38] and subsequent accounts on work with this measurement system carried out under NSF sponsorship[5,25,32] have included comparisons of EL2 maps with those for dislocation density and MESFET parameters in the same wafers.

While recognizing the instantaneous nature of the qualitative but useful information about EL2 distribution on a macro- and micro-scale that can be achieved with an infrared microscope using a vidicon viewer, our work has not emphasized that aspect of wafer mapping, for two reasons: it has not been up to now quantitative (though Samuelson at the University of Lund is working on that), and it is usually difficult to get enough discrimination unless the sample is several mm thick. The line-scanning method of Windschief et al.[37] which uses a multi-element array of silicon detectors has been able to

achieve absorption discrimination with wafers down to 0.5 mm thickness (though it could not when that group first claimed to be able to do so!), but is able to measure only the absorption coefficient referenced to that of a second wafer (which is kept out of focus so as not to impose any non-existent spatial features on the computer-printed map of the subject wafer. We have, in fact, provided absolute calibrations of two GaAs wafers at several wavelengths for that group at the Fraunhofer Institute in Freiburg, which they can then use as their "reference standards".

By elimination, we have adopted the point-by-point scanning method, using a stationary optical path that includes a region on the wafer some 0.5 mm in diameter. A computer control moves the wafer laterally with respect to that optical path, so that transmittance values for some 2000 locations can be acquired and stored on disc in a 20 minute measurement sequence, these involving determination of the transmittance to some 0.03%. That allows us to determine the neutral EL2 concentration N° in a 0.5 mm thick wafer with a resolution $\Delta N \approx 10^{14}$ cm^{-3}. Since N° for SI LEC GaAs is usually at least 2×10^{15} cm^{-3}, more typically from four to six times that much, and sometimes as large as 3×10^{16} cm^{-3}, we are able to detect quite subtle changes in N° over the area of a wafer in which this property happens to be rather uniform. The measurement system we use is illustrated in Figure 7, and further details are described elsewhere.[32]

Despite the high sensitivity of our system, even this does have limits, and we were obliged to report a negative result on

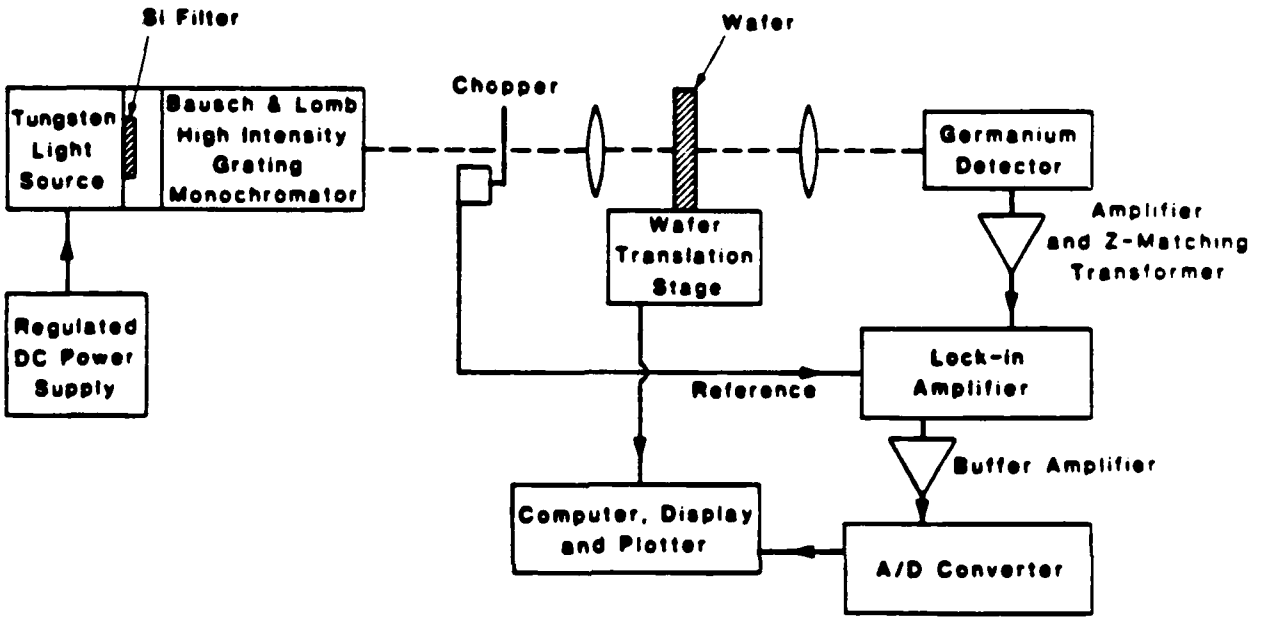


Figure 7. Schematic of the system used at the Oregon Graduate Center for measurement of neutral EL2 density (N°), from the near-IR transmittance. The wavelength used for measurement is selected normally to be 1.0 or 1.1 μm, though for samples with very small N° the sensitivity can be further enhanced by measurement at a shorter wavelength (down to 920 nm).

one aspect of our EL2 mapping work. This concerned a request by DARPA and by ARACOR, Inc. of Sunnyvale, California (a DARPA contractor) to attempt observation of a change in the near-IR transmittance attributable to the kind of surface treatment (a chemo-mechanical noncontact polish) applied to GaAs samples at ARACOR. Over a substantial period of time, we measured and mapped the near-IR transmittance of GaAs slabs (with thickness up to 5 mm) and much thinner wafers, before and after the ARACOR process had been used.

If indeed the lapping/polishing methods used by commercial GaAs producers does cause substantial sub-surface damage, one might indeed hope that measurement of GaAs before and after ARACOR's removal of that damaged layer would lie above the lower limit of detectivity. However, we were not able to detect whatever small change in transmittance would be associated with removal of that affected material. (Of course, the optical density of such a treated wafer did change, since it was less thick at the second measurement.) Figure 8 serves as a summary of what we found; the deduced N° was the same for the ARACOR-treated and untreated portions of a Spectrum Technology SI LEC wafer. The negative result obtained for this 0.6 mm thick GaAs (as for other samples we measured to assist ARACOR and DARPA in this study) was frustrating to the ARACOR staff, but not really surprising, since any sub-surface damage of different opacity would be expected to be much thinner than the full wafer thickness.

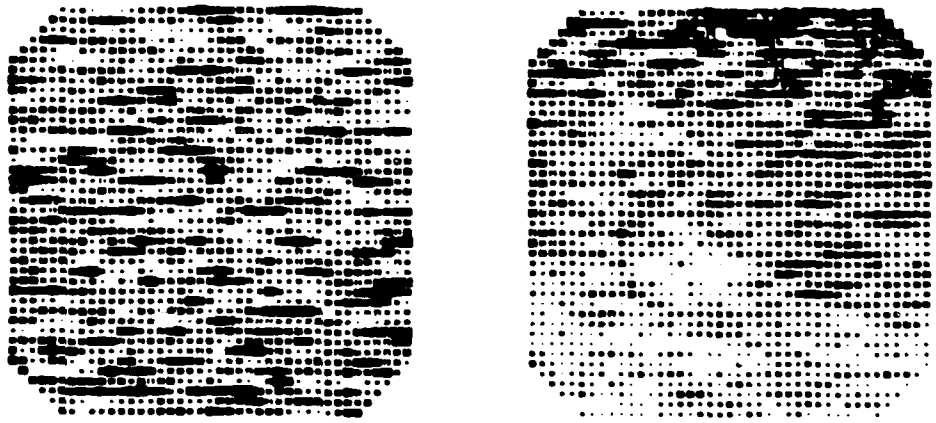


Figure 8. Transmission data (converted to a grey-scale plot representation of the apparent neutral EL2 density N° in two portions of a (Spectrum Technology) SI GaAs wafer grown by low-pressure LEC. The right-hand part of the figure shows results for a portion having received ARACOR's "non-contact polishing" treatment.

Allowing for the slightly different thicknesses of these two pieces of GaAs, the mean value deduced is $\bar{N}° = 9 \times 10^{15}$ cm^{-3} in both cases. Thus (for a sample of thickness 0.6 mm) any change in optical density caused by the ARACOR treatment is not detectable.

As an example of successful work with EL2 measurement carried out to assist DARPA-supported work, Figures 9 and 10 show maps of N° for two SI LEC GaAs wafers grown at Westinghouse Research and Development Center. Wafer BN106#16, for which Figure 9 shows the variations of N°, evidently came from near the seed end of an "undoped" ingot (we presume Wafer #16 of Crystal BN106); the EL2 concentration has a satisfactory degree of uniformity (±5% excursions about the mean $\bar{N}° = 5.8 \times 10^{15}$ cm^{-3}), and there is slight evidence of the four-fold symmetric pattern resulting from strain anisotropy in the cooling crystal.[29]

Figure 10 shows the corresponding N° map for a wafer from one of the indium-alloyed SI LEC GaAs crystals grown at Westinghouse. Apart from the customary indication of a (011) flat, this wafer was not fully round - though more nearly so than indicated in the plot itself. We were not advised as to the dislocation density in this In-doped material - and have not yet had the temerity to etch it to expose dislocation etch pits; preferring first to obtain other nondestructive tests, then get devices made and measured, before embarking on the irreversible step of etching with KOH. However, we were advised by Dr. McGuigan of Westinghouse that this material <u>is</u> semi-insulating, and that it received a post-growth anneal. Observe that despite a presumably low to zero dislocation density, N° is moderately large: $\bar{N}° = 7.2 \times 10^{15}$ cm^{-3}, some 20% larger than in the sample of Figure 9. Observe also that, for reasons not yet understood, the spread of N° values is rather larger in this case. There is

Map of Near-IR Absorbance/EL2 Concentration N°, for Semi-Insulating Westinghouse Undoped LEC Wafer BN106#16.(d = 50 mm, t = 0.53 mm)

Measured at 300 K, and λ = 1.00 μm.

Average neutral EL2, $\bar{N}° \simeq 5.8 \times 10^{15}$ cm^{-3}, with ± 5% excursions.

Max. shading ■ where $N° > 6.0 \times 10^{15}$ cm^{-3} ($\alpha > 0.72$ cm^{-1})

Zero shading where $N° \quad 5.6 \times 10^{15}$ cm^{-3} ($\alpha < 0.68$ cm^{-1})

Four intermediate shadings used with interval $\Delta N° = 1 \times 10^{14}$ cm^{-3}.

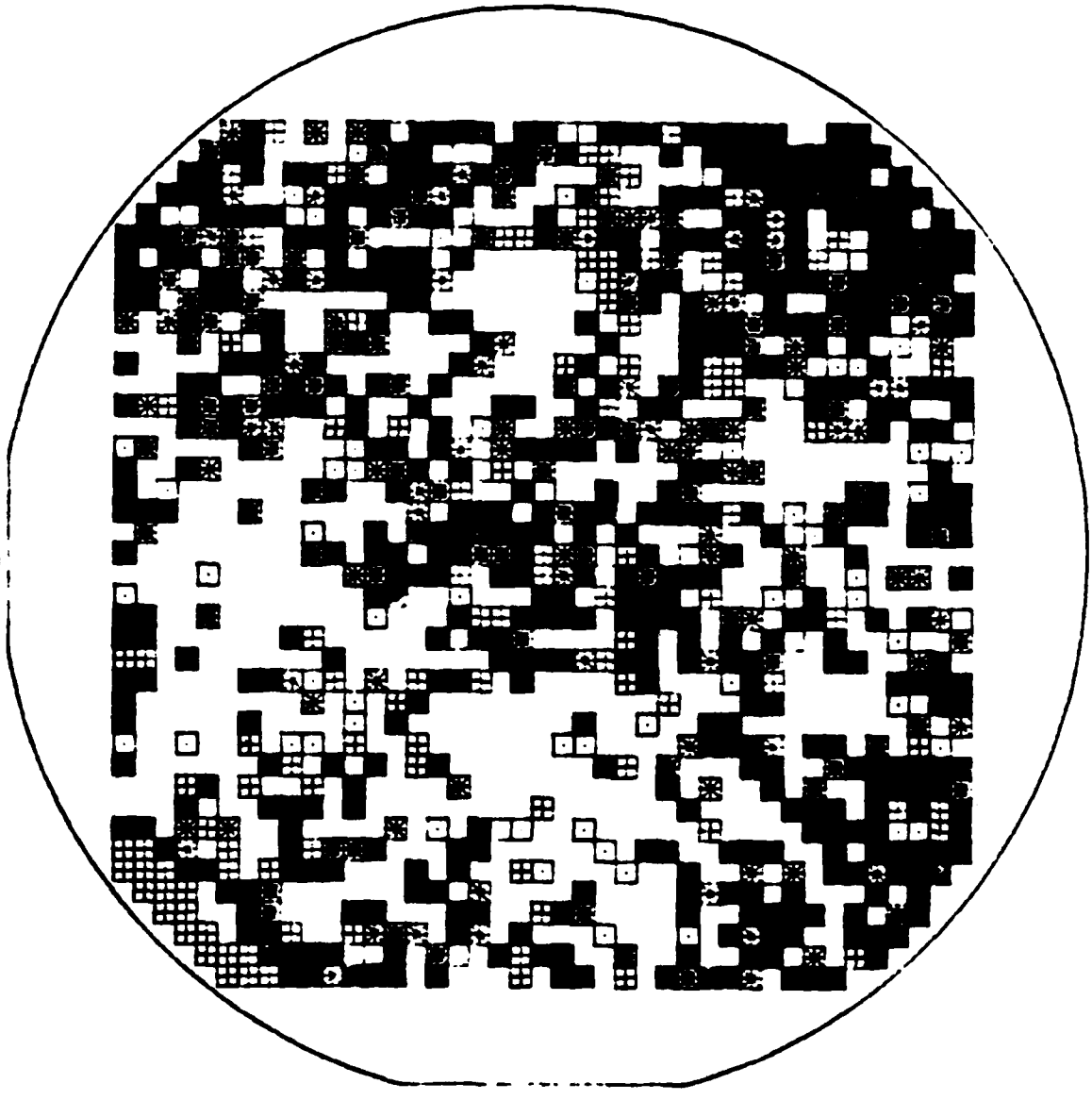


Figure 9

Map of Near-IR Absorbance/EL2 Concentration N°, for Semi-Insulating Westinghouse In-Doped LEC Wafer BN109#82 (t = 0.58 mm, area slightly flattened from a full 50 mm circle. The actual area does extend somewhat beyond the two lines drawn below.)

Measured at 300 K, and at $\lambda = 0.95\ \mu m$.

Average neutral EL2, $\bar{N}^\circ = 7.2 \times 10^{15}\ cm^{-3}$, with a few areas up to 13% above that average. (The shading scheme below leaves areas of average N° blank.)

Max. shading ■ where $N^\circ > 8.3 \times 10^{15}\ cm^{-3}$ ($\alpha > 1.16\ cm^{-1}$)

Zero shading where $N^\circ < 7.5 \times 10^{15}\ cm^{-3}$ ($\alpha < 1.04\ cm^{-1}$)

with four intermediate degrees of shading used, interval $\Delta N^\circ = 2.25 \times 10^{14}\ cm^{-3}$.

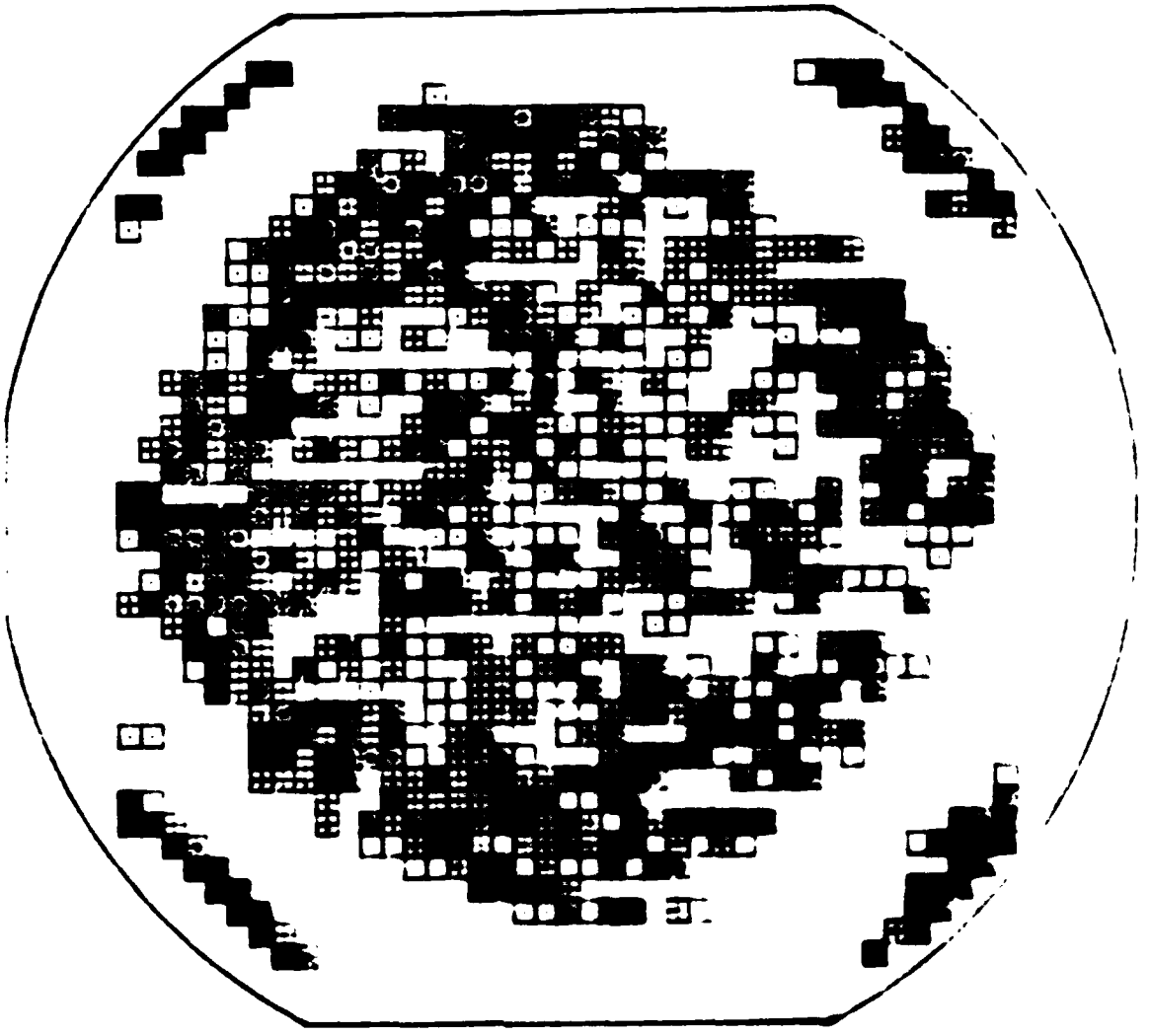
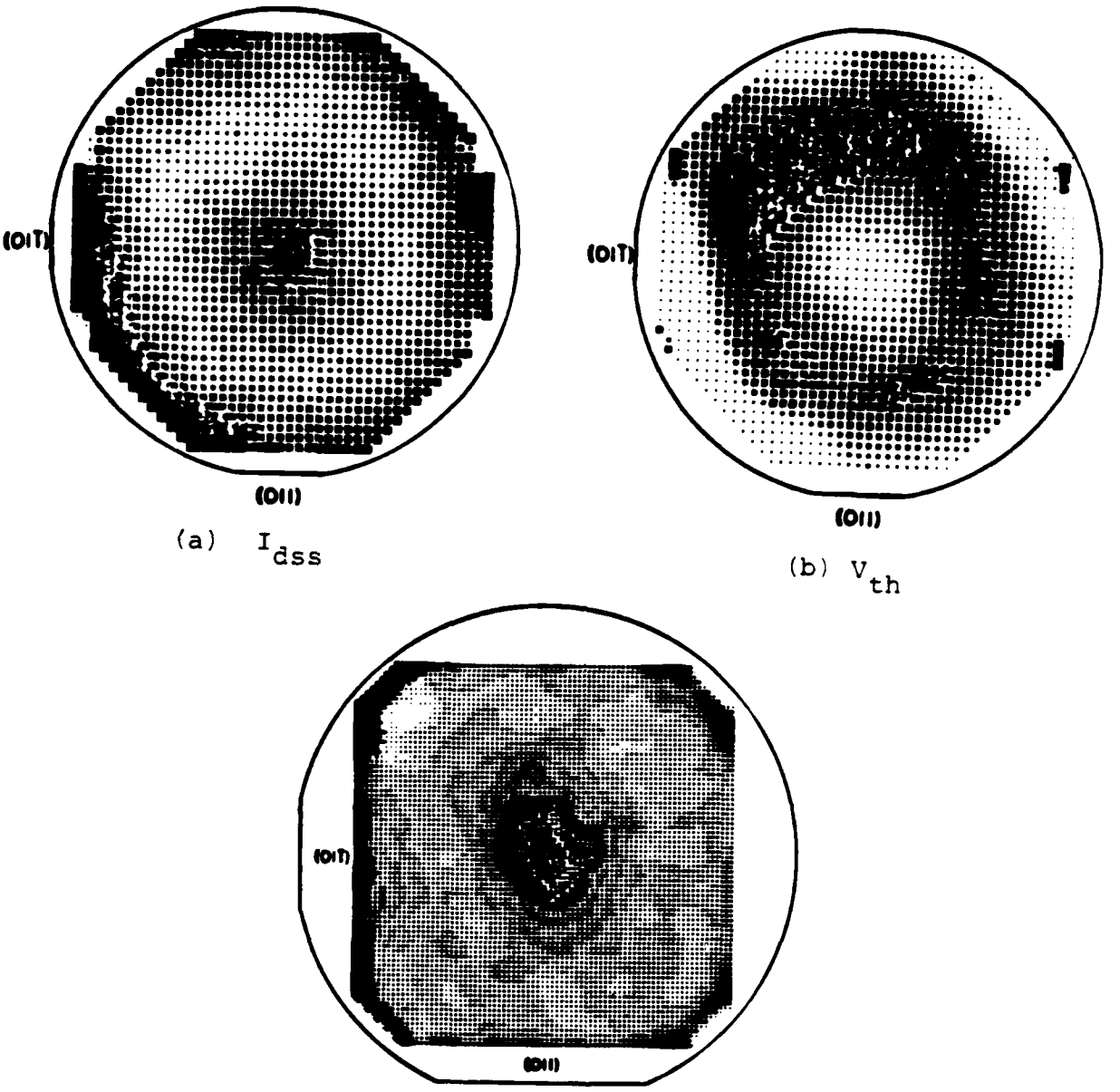


Figure 10.

clearly a need for further study of the effects of both post-growth heat treatment, and of indium-alloying, on the resulting spatial distribution and mean value of EL2.

This final section of the Report concludes with a brief account of work we have carried out in collaboration with Tri-Quint Semiconductor of Beaverton, to compare measurements of EL2 N°, dislocation density N_D, and parameters of direct-implant MESFET devices such as V_{th} and I_{dss}. While this work was not directly sponsored by DARPA, it is closely linked with the views expressed in various earlier pages of this Report, that full success in implementing high-performance high-speed GaAs devices depends on a fuller understanding of how material and device properties are related.

Figure 11 shows N°, V_{th}, and I_{dss} mapped for a 50 mm wafer of Cominco SI GaAs, coming from near the tail end of a high-pressure LEC ingot. As an important adjunct to the maps of Figure 11, it should be noted that, subsequent to the fabrication and measurement of enhancement mode FETs and other devices in this wafer (done at Triquint), we destroyed those devices as an inevitable consequence of immersing the wafer in molten KOH to determined the magnitude and spatial variation of N_D. To our surprise, N_D in this wafer, while large ($\sim 2 \times 10^5$ cm^{-2}) was essentially uniform. Thus changes in device parameter could not be linked directly to the proximity or non-proximity of a dislocation. Yet there was a distinctive spatial pattern for the device values of I_{dss} and V_{th}, which Figure 11 shows to be significantly correlated with variations of EL2 N°. Indeed,



(a) I_{dss}

(b) V_{th}

(c) EL2 N°

Figure 11. An example of interproprty comparison for a SI LEC GaAs wafer, grown by Cominco. Parts (a) and (b) show properties for enhancement MESFETs. (a) I_{dss}, with each stage of darkening meaning a 1% increase. (b) V_{th} with the lighter areas being more negative. (c) The pattern of N° measured prior to device fabrication by near-IR transmittance , averaging $\bar{N}° = 8 \times 10^{15}$ cm^{-3}, with ±20% variations. Note that V_{th} is most negative where EL2 centers are most numerous.

a correlation plot of V_{th} or I_{dss} with N° for this wafer shows a correlation with a >99% significance.[25]

This does not, of course, mean that dislocations have no effect on device properties, but it does show that the local EL2 concentration affects the FET channel characteristics, presumably through the space charge of EL2 sites at the channel/substrate interface. For some other wafers, we have seen N°, N_D, and device parameters <u>all</u> showing the same spatial pattern, such as the familiar stress/dislocation four-fold pattern described by Jordan from thermoelastic considerations.[29]

At the conclusion of this DARPA contract, we are continuing to measure and map EL2, and to collaborate with others concerning measurements and analyses that various groups can do best. Our collaboration with TriQuint on devices continues, and we have measured "undoped" and "indium doped" wafers from a wide variety of US, European and Japanese commercial suppliers, from which we eventually hope to find further correlations between materials and device properties.

REFERENCES

(Other than the items concerning electron velocity effects listed on pages 10 through 44.)

1. J. S. Blakemore, "Semiconducting and Other Major Properties of Gallium Arsenide," J. Appl. Phys. 53, R123 (1982).
2. G. M. Martin, A. Mitonneau and A. Mircea, "Electron Traps in Bulk and Epitaxial GaAs Crystals," Electron. Lett. 13, 191 (1977).
3. A. Mircea, A. Mitonneau, L. Hollan, and A. Brière, "Out-diffusion of Deep Electron Traps in Epitaxial GaAs," Appl. Phys. 11, 153 (1976).
4. G. A. Baraff and M. Schlüter, "Electronic Structure, Total Energies and Abundances of the Elementary Point Defects in GaAs," Phys. Rev. Lett. 55, 1327 (1985).
5. J. S. Blakemore and P. Dobrilla, "Factors Affecting the Spatial Distribution of the Principal Midgap Donor in Semi-Insulating Gallium Arsenide Wafers," J. Appl. Phys. 58, 204 (1985).
6. W. B. Leigh, J. S. Blakemore, and R. Y. Koyama, "Interfacial Effects Related to Backgating in Ion-Implanted GaAs MESFETs," IEEE Trans. Electron Dev. ED-32, 1835 (1985).
7. Inst. Phys. Conf. Ser., Nos. 45 (1979), 56 (1981), 63 (1982), 65 (1983), and 74 (1985).
8. "Semi-Insulating III-V Materials: Nottingham 1980," edited by G. J. Rees (Shiva, 1980), 361 pp.

9. "Semi-Insulating III-V Materials: Evian 1982," edited by S. Makram-Ebeid and B. Tuck (Shiva, 1982), 397 pp.

10. "Semi-Insulating III-V Materials: Kah-nee-ta 1984," edited by D. C. Look and J. S. Blakemore (Shiva, 1984), 504 pp.

11. S. Makram-Ebeid, P. Langlade, and G. M. Martin, "Nature of EL2: the Main Native Midgap Electron Trap in VPE and Bulk GaAs," in Ref. 10 (1984), p. 184.

12. M. Baeumler, U. Kaufmann, and J. Windschief, "Photoresponse of the As_{Ga} antisite defect in as-grown GaAs," Appl. Phys. Lett. 46, 781 (1985).

13. M. Kaminska, "Defect Identification: EL2 in GaAs," in Proc. 17th Internat. Conf. on Physics of Semiconductors (Springer-Verlag, 1985), p. 741.

14. M. Deiri, K. P. Homewood, and B. C. Cavenett, "Identification of EL2 in GaAs as the As_{Ga} Antisite Centre," J. Phys. C. 17, L627 (1984).

15. B. K. Meyer and J-M. Spaeth, "As_{Ga} Antisites and Their Relation to EL2 Defects in GaAs," J. Phys. C 18, L99 (1985).

16. M. Taniguchi, Y. Mochizuki, and T. Ikoma, "Photoquenching Effect at the Midgap Electron Traps (EL2 Family) in Different GaAs Crystals," in Ref. 10 (1984), p. 231.

17. G. M. Martin, at 5th "Lund" Deep-Level Impurity Conf., St. Andrews, Scotland (June 1985) (unpublished).

18. G. M. Martin and S. Makram-Ebeid, "Manifestations of Deep Level Point Defects in GaAs," Physica 116B, 371 (1983).

19. R. D. Fairman and J. R. Oliver, "Growth and Characterization of Semi-Insulating GaAs for Ion Implantation," in Ref. 8 (1980), p. 83.

20. S. Miyazawa, Y. Ishii, S. Ishida, and Y. Nanishi, "Direct Observation of Dislocation Effects on Threshold Voltage of a GaAs Field-Effect Transistor," Appl. Phys. Lett. 43, 853 (1983).

21. Y. Ishii, S. Miyazawa, and S. Ishida, "Threshold Voltage Scattering of GaAs MESFETs Fabricated on LEC-Grown Semi-Insulating Substrates," IEEE Trans. ED-31, 800 (1984).

22. H. Yamazaki, T. Honda, S. Ishida, and Y. Kawasaki, "Improvement of FET Threshold Voltage Uniformity by Using Very Low Dislocation Density LEC Czochralski-Grown GaAs," Appl. Phys. Lett. 45, 1109 (1984).

23. Y. Nanishi, S. Miyazawa, and Y. Matsuoka, "Homogeneity Correlation between GaAs Crystal Parameters and FET Performance", to appear in Proc. Internat. Symp. on Defect Recognition and Image Processing (North-Holland, 1986).

24. H. V. Winston, A. T. Hunter, H. M. Olsen, R. P. Bryan, and R. E. Lee, "Substrate Effects on the Threshold Voltage of GaAs Field Effect Transistors," Appl. Phys. Lett. 45, 447 (1984).

25. P. Dobrilla, J. S. Blakemore, A. J. McCamant, K. R. Gleason, and R. Y. Koyama, "GaAs FET Properties, as Influenced by the Local Concentrations of Midgap Native Donors and Dislocations," Appl. Phys. Lett. 47, 602 (1985).

26. G. Jacob, "How to Decrease Defect Densities in LEC SI GaAs and InP Crystals," in Ref. 9 (1982), p. 2.

27. H. M. Hobgood, R. N. Thomas, D. L. Barrett, G. W. Eldridge, M. M. Sopiro, and M. C. Driver, "Large Diameter Low Dislocation In-doped GaAs: Growth, Characterization, and Implications for FET Fabrication," in Ref. 10 (1984), p. 149.

28. J. Osaka and K. Hoshikawa, "Homogeneous GaAs Grown by Vertical Magnetic Field Applied LEC Method," in Ref. 10 (1984), p. 126.

29. A. S. Jordan, R. Caruso, and A. R. Von Neida, "A Thermoelastic Analysis of Dislocation Generation in Pulled GaAs Crystals," Bell Syst. Tech. J. 59, 593 (1980).

30. H. Ehrenreich and J. P. Hirth, "Mechanism for Dislocation Density Reduction in GaAs Crystals by Indium Addition," Appl. Phys. Lett. 46, 668 (1985).

31. G. M. Martin, "Optical Assessment of the Main Electron Trap in Bulk Semi-Insulating GaAs," Appl. Phys. Lett. 39, 747 (1981).

32. P. Dobrilla and J. S. Blakemore, "Experimental Requirements for Quantitative Mapping of Midgap Flaw Concentration in SI GaAs Wafers by Measurement of Near-IR Transmittance," J. Appl. Phys. 58, 208 (1985).

33. R. T. Chen, D. E. Holmes, and P. M. Asbeck, "Correlation of Threshold Voltage of Implanted Field Effect Transistors and Carbon in GaAs Substrates," Appl. Phys. Lett. 45, 459 (1984).

34. D. Rumsby, I. Grant, M. R. Brozel, E. J. Foulkes, and R. M. Ware, "Electrical Behavior of Annealed LEC GaAs," in Ref. 10 (1984), p. 165.

35. S. Martin, M. Duseaux, and M. Erman, "Distribution of EL2 in Dislocated and Dislocation-free GaAs Substrates Before and After Annealing," Inst. Phys. Conf. Ser., No. 74, 53 (1985).

36. S. Martin and M. Duseaux, "Kinetics of LEC GaAs Properties under Annealing," to appear in Proc. Internat. Symposium on Defect Recognition and Image Processing in III-V Compounds (North-Holland, 1986).

37. J. Windschief, M. Baeumler, and U. Kaufmann, "Near Infrared Transmission Imaging of Spatial Inhomogeneities in GaAs Slices - a Comparative Study of Different Techniques," same volume as Ref. 36 (North-Holland, 1986).

38. P. Dobrilla, J. S. Blakemore, and R. Y. Koyama, "Quantitative Mapping of EL2 Concentration Across SI GaAs Wafers from Infrared Transmittance Data," in Ref. 10 (1984), p. 282.